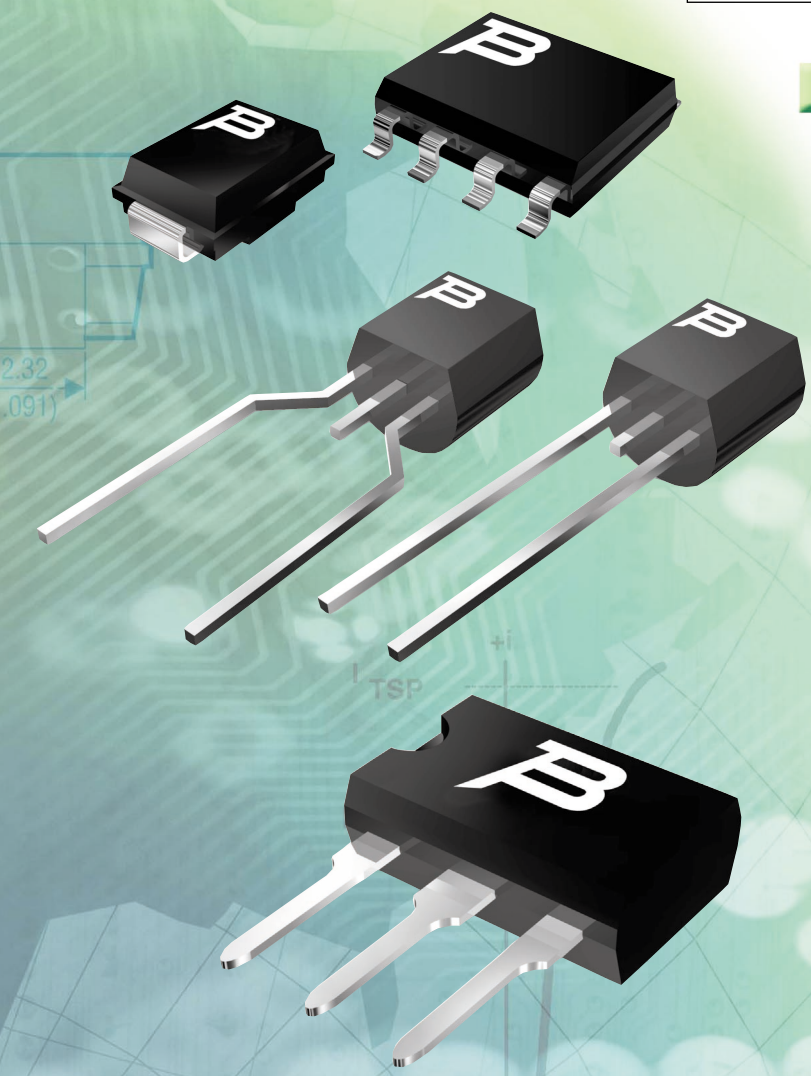


TISP®

Telecom Overvoltage Protectors

Introduction

This section covers the overvoltage protection functions and Bourns TISP® (Totally Integrated Surge Protector) thyristor SPDs (Surge Protective Devices) in terms of evolution, function, silicon structure, electrical characteristics, electrical rating and device variants.

Basic Protection Function

SPDs have a non-linear voltage-current characteristic which limits overvoltages by diverting the current caused by an overvoltage. Figure 1 shows how a two-terminal SPD is applied to limit the voltage between two conductors and one conductor and ground. There are two basic types of SPD characteristics; clamping and switching.

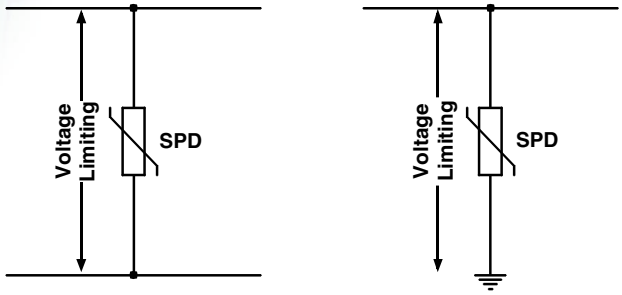


Figure 1. SPD Circuit Application

Clamping SPDs have a continuous voltage-current characteristic - Figure 2. In limiting an overvoltage, the downstream load will be exposed to a high voltage for the time period that the overvoltage exceeds the system rated voltage level - see Figure 2 waveshape. Obviously it is important that normal system voltages are not clamped.

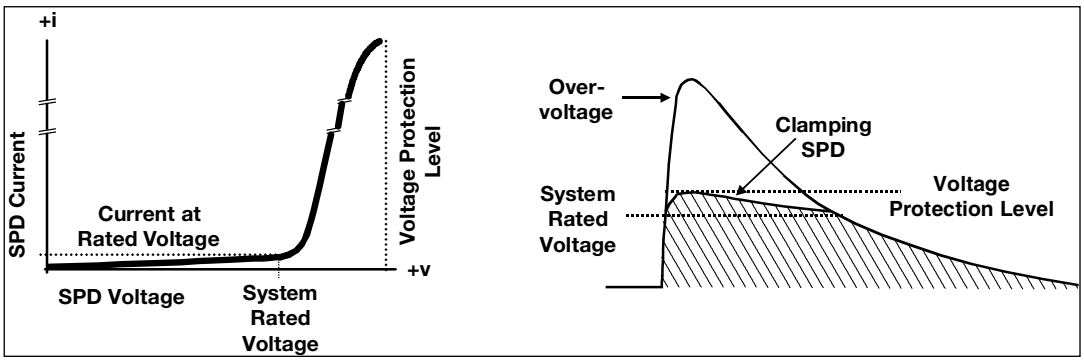


Figure 2. Clamping SPD Characteristic and Voltage Limiting Waveshape

Switching SPDs have a discontinuous voltage-current characteristic, the discontinuity being caused by the switching action between high voltage and low-voltage regions. The TISP® device has a switching characteristic as it is a thyristor device. Before the TISP® device switches into a low voltage state, there is a small clamping action, caused by the breakdown region - see Figure 3. In limiting an overvoltage, the downstream load will be exposed to a high voltage for the brief time period that the TISP® device is in the breakdown region before switching into a low-voltage state - see Figure 3 waveshape. When the diverted current falls below a critical value, the TISP® device switches off and allows normal system operation to resume.

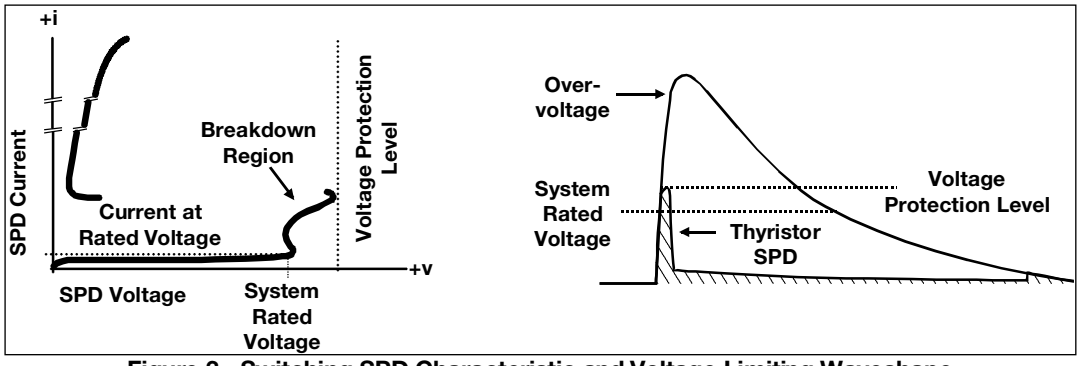


Figure 3. Switching SPD Characteristic and Voltage Limiting Waveshape

TISP® Origination

In 1980, British Telecom announced the development of a new generation of telephone exchanges called "System X" which would employ the latest semiconductor devices. Lightning, a.c. power system faults and switching produce voltages on the telephone line. The ICs which directly interfaced to the telephone line would be exposed to such voltages and needed accurate and fast overvoltage protection to prevent failure. It had been established that the best type of SPD for this application was thyristor based. However, at that time, the thyristor SPDs available would only protect in one voltage polarity. Protection in both voltage polarities and both line conductors would require four devices. System X designers asked several thyristor manufacturers if the protection for one line could be integrated into one package.

Bourns' Bedford semiconductor power device facility met this challenge. Being an established thyristor manufacturer meant that the basic thyristor structure already existed. However, how to integrate four devices, achieve a 30 year life and accurate voltage control required the initiation of a major research and development program. The need for integration and long life was solved by the adoption of a planar structure, and accurate voltage control was achieved through the use of a buried ion-implanted layer (UK patent 2113907, 1981). Production of these devices started in 1982 and, today, both fixed voltage and gated products are produced. The following clauses give more detail on the make up of a fixed voltage TISP® device.

Basic Thyristor Structure

Figure 4 shows the simplified structure of a unidirectional thyristor protector. The switching action occurs when the top contact is negative with respect to the bottom contact. Also shown are the equivalent circuit elements created by the semiconductor layers. Typically, the protector would be manufactured starting with an n^- wafer. Layers of p material would then be diffused into the top and bottom. Next, n^+ regions would be diffused into the top surface. Finally, the top and bottom would be metallized to provide contacts.

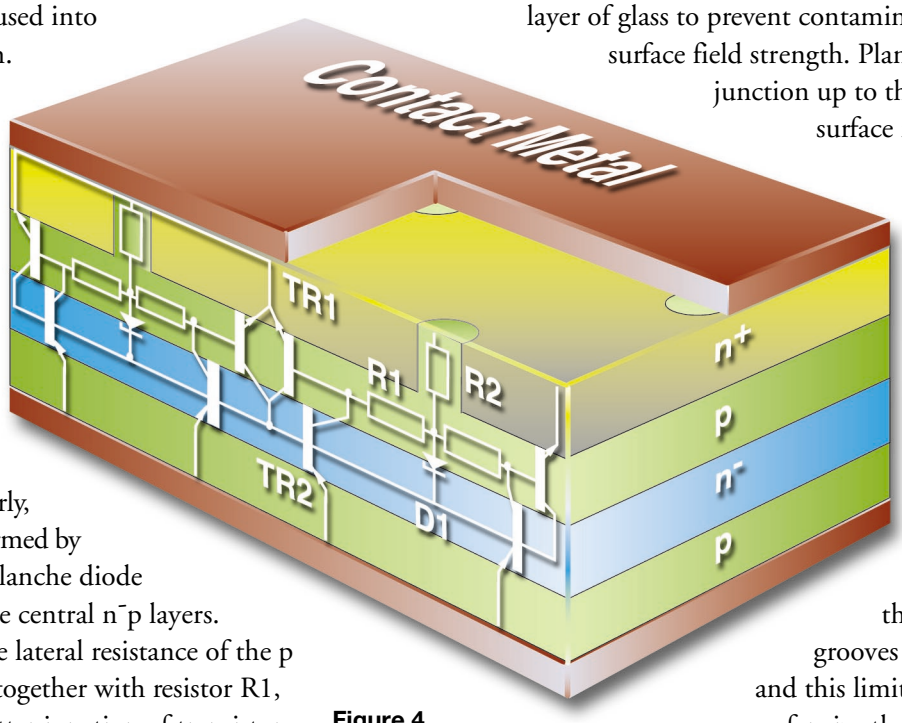


Figure 4.
Simplified Protector Structure

Transistor TR1 is formed by the n^+pn^- layers. Similarly, transistor TR2 is formed by the pn^-p layers. Avalanche diode D1 is formed by the central n^-p layers. Resistance R1 is the lateral resistance of the p layer. Resistor R2, together with resistor R1, shunt the base-emitter junction of transistor TR1 to define the value of switch-off current. Resistor R2 has a relatively low value of resistance and is considered as a local base short to the emitter. In manufacture, the emitter diffusion is perforated with a series of dots to create these shorts. In Figure 4, some of the top metallization has been omitted to show the p-type dots. The practical implementation of this structure requires technology decisions on how the protection voltage is set and the surface termination of the voltage blocking junctions.

Junction Termination

The technology used for junction termination at the chip surface was decided by future needs and performance history. Three common ways of controlling junction breakdown at the surface are shown in Figure 5. Glassed Mesa technology terminates the high voltage junction on the edge of a mesa created by grooving the silicon wafer. The mesa is sealed with a layer of glass to prevent contamination and reduce the surface field strength. Planar brings a lateral junction up to the top surface. The surface is sealed with silicon dioxide in the junction area. Additional stability is provided by a channel stopper diffusion.

Although the double sided glass mesa gives the smallest chip size, the double mesa grooves weaken the wafer and this limits the maximum wafer size that can be processed without excessive breakage. Single glass mesa and planar solve these problems at the expense of increased chip size used to bring the lower junction up to the top surface. The mesa groove still limits the maximum wafer size. Planar does not have any wafer size limitation. Both these technologies were established in production at Bedford.

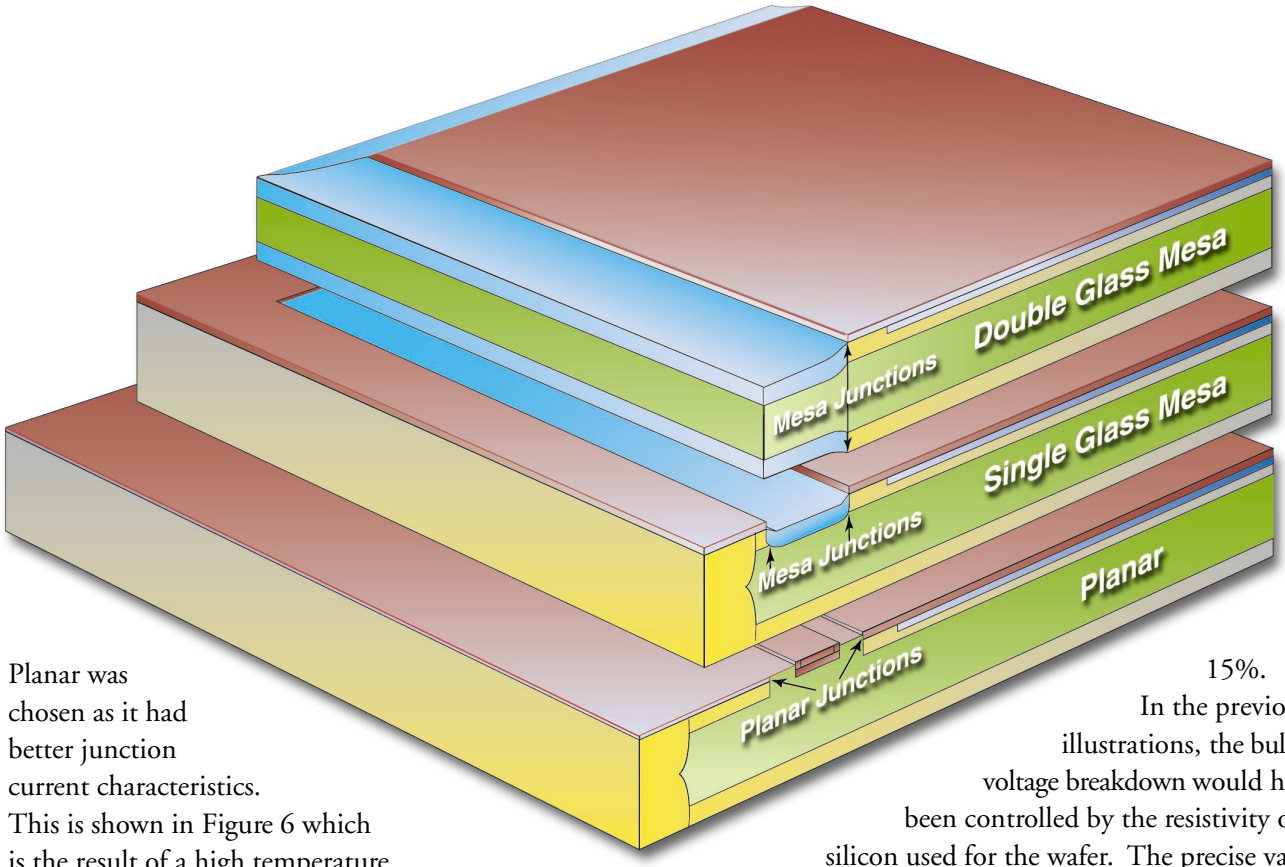


Figure 5.
Junction Termination Technologies

Planar was chosen as it had better junction current characteristics. This is shown in Figure 6 which is the result of a high temperature reverse biased (HTRB) life test on high voltage glass mesa and planar transistors. An advantage of the planar structure approach is that multiple protectors may be easily made on a single chip. Each protector is formed in a wraparound of p-type silicon, which serves to isolate the protector sections from each other.

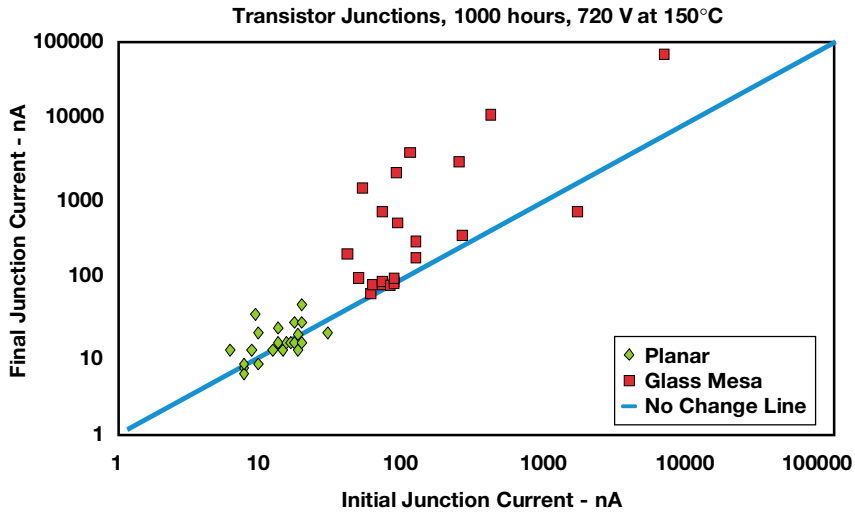


Figure 6. Junction Current Stability

Voltage Accuracy

Protectors have to be supplied to a specified voltage window; that is a maximum and minimum value of breakdown voltage. This window might be as little as 15%.

In the previous illustrations, the bulk voltage breakdown would have been controlled by the resistivity of the silicon used for the wafer. The precise value of resistivity will vary across a wafer, from wafer to wafer and from lot to lot. Using starting wafer resistivity for determining the breakdown voltage could create yield consistency problems on tight voltage windows.

An alternative approach is to use a high resistivity silicon wafer which would give a higher breakdown voltage than required, and diffuse in a lightly doped layer which lowers the breakdown voltage to the required value. In order to be successful, the doping of this additional layer needs to be highly accurate.

Ion-Implantation is needed to give sufficient precision in controlling the level of dopant. Lowering the silicons' breakdown voltage by diffusion allows selective breakdown areas. A pad of dopant can be implanted at the centroid of each emitter. Breakdown will occur at this pad, which will be deep in the bulk of the silicon and well away from the chip surface. By defining the breakdown region, the switch-on and current spreading performance should be more consistent.

The use of a breakdown pad considerably reduces the breakdown voltage sensitivity to surface states. Chip surface voltage control will still be required, but the chances of premature surface breakdown are now considerably reduced. Figure 7 shows a typical TISP® device structure which uses a buried breakdown pad and planar junction termination. This structure shows a 1988 development of the original ion-implanted patent and is covered by US patent number 4,967,256.

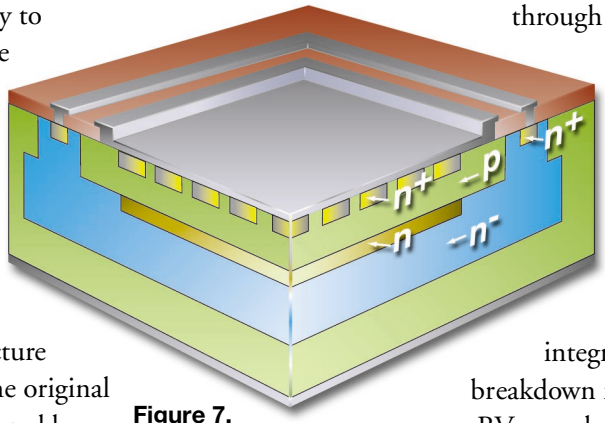
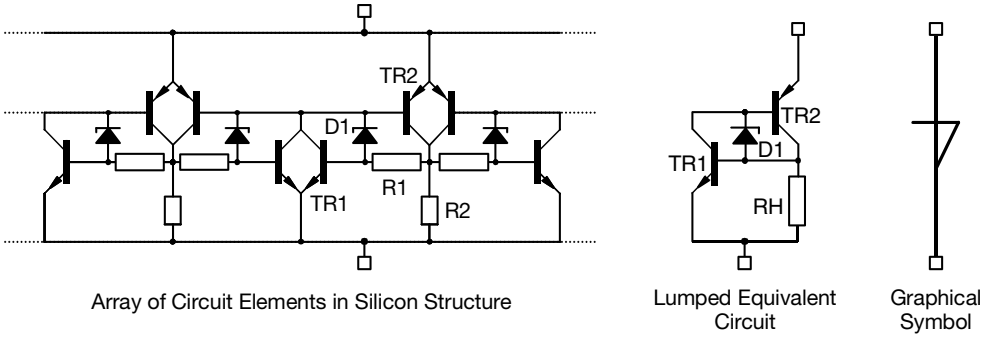


Figure 7.
Typical TISP® Structure

Simple Equivalent Circuit

The array of circuit elements shown in Figure 4 can be simplified to a lumped equivalent circuit containing a transistor pair, TR1 and TR2, an avalanche diode, D1, and a shunt resistor, RH. Figure 8 shows these two circuits together with the graphical symbol for the protection structure.



Array of Circuit Elements in Silicon Structure

Lumped Equivalent Circuit

Graphical Symbol

Figure 8. Protector Circuits and Symbol

Protection Characteristics

The voltage-current characteristic of the protector can be explained using the lumped equivalent circuit of Figure 8. Figure 9 shows the protector voltage-current characteristic together with the parts of the lumped equivalent circuit that are carrying significant current during each of the various operating modes.

In the off-state condition, when the voltage is increased from zero in the positive polarity, most of the voltage is supported by the (reversed biased) collector-base junction of transistor TR2. The current path is through transistor TR2, and resistor RH. The current levels are very low during this condition as shown in Figure 6.

The breakdown region initiates when the applied voltage is sufficient to cause the diode D1, to avalanche. As the diode D1 is integrated with transistor TR2, the breakdown region is a classic transistor BV_{CEO} shape. After the initial breakdown, the characteristic is re-entrant as the transistor gain increases and then the characteristic shows a positive slope characteristic at higher current levels. The current path is through the emitter of transistor TR2, then through the parallel combination of the transistor collector-base and diode D1, and exits through resistor RH.

When the voltage developed across resistor RH, is sufficient to cause the conduction of transistor TR1, its collector draws extra current from the base of transistor TR2. The extra base current causes transistor TR2, to pass more base current into transistor TR1. A regenerative transistor pair is formed. The breakdown characteristic develops a negative slope and the characteristic terminates when the transistors pass enough current to switch into a low voltage on state.

In the low voltage state and at high current, the transistors will pass most of the current. As the current reduces, the current taken by resistor RH, shunting the base emitter of transistor TR1, becomes significant. Switch off occurs when the current level falls to a point where the voltage developed across the resistor RH, the transistor TR1, base-emitter voltage, is less than the value needed to cause transistor conduction and the transistor pair switches off.

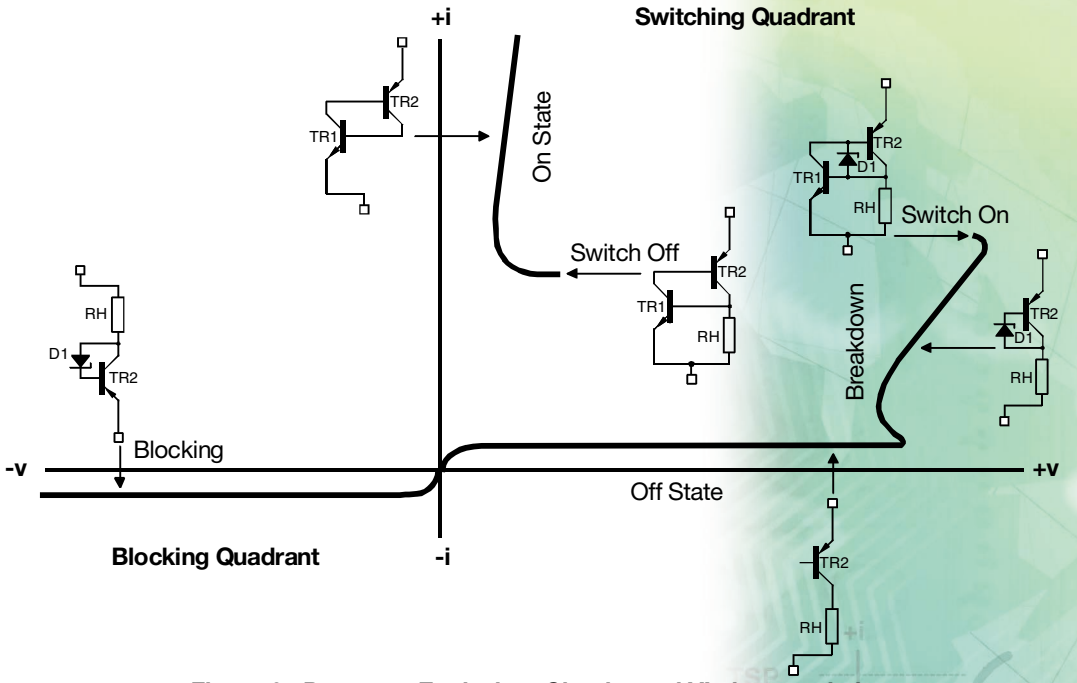


Figure 9. Protector Equivalent Circuits and VI characteristic

In the opposite voltage polarity, most of the voltage is supported by the reverse biased base-emitter of transistor TR2. In this blocking condition, the current path is through transistor TR2, and resistor RH.

This protector has a switching characteristic in the positive polarity and a blocking characteristic in the negative polarity. For this reason it is called a unidirectional protector - the switching characteristic only occurs in one polarity. It can be further qualified as a reverse blocking unidirectional protector. Figure 10 shows the characteristic and symbol for the reverse blocking unidirectional protector. Note that the reverse blocking capability is higher than the positive polarity breakdown voltage.

A bidirectional protector can be made by integrating a similar unidirectional protector in antiparallel - Figure 11. When one unidirectional protector is in its switching polarity, the other will be blocking. Similarly, by integrating a diode in antiparallel, a forward conducting unidirectional protector can be made - Figure 11. Although this protector passes high currents in both voltage polarities, it is still called unidirectional as there is only one switching quadrant. The bottom pair of characteristics in Figure 11 shows the blocking characteristics of the paralleled sections for information only. The switching and diode conduction characteristics will mask out the blocking characteristics on the actual protector characteristic.

Three protection structures are the building blocks for fixed voltage TISP® SPDs; the reverse blocking unidirectional, the forward conducting unidirectional and the bidirectional.

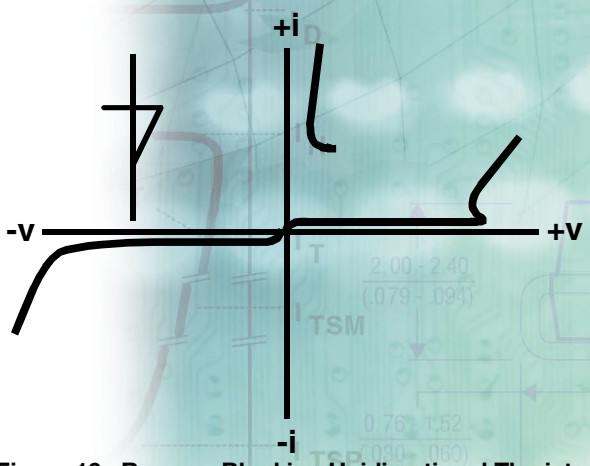


Figure 10. Reverse Blocking Unidirectional Thyristor

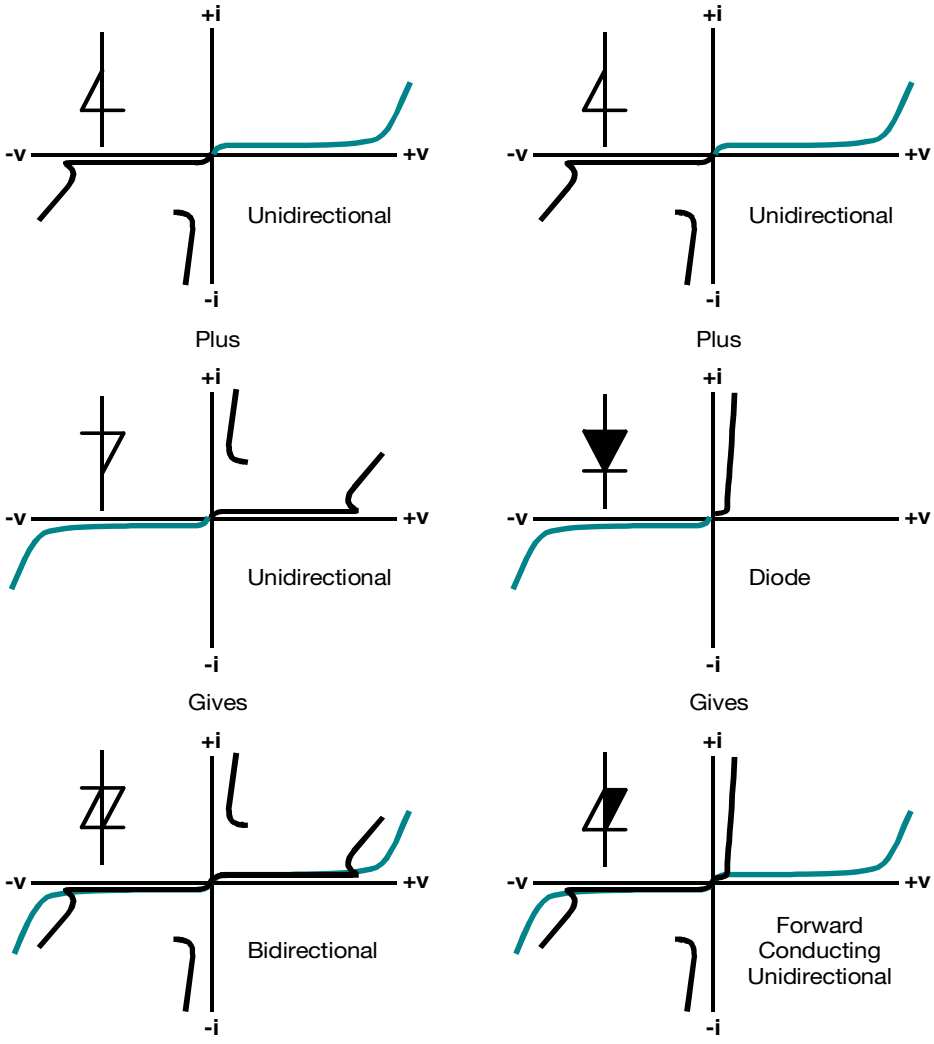


Figure 11.
Formation of Bidirectional and Forward Conducting Unidirectional Protectors by Antiparallel Connection

TISP® Electrical Requirements and Terms

Figure 12 shows the switching characteristic of Figure 9 annotated with parameter letter symbols. In service, the TISP® device must meet requirements in three areas:

Transparency - The normal system operation must not be degraded
Protection - Under the specified overstress conditions, the protected equipment performs as required without creating hazards
Durability - Provide reliable long term transparency and protection

Transparency

The protector's off-state current and the capacitance must not affect the signals normally occurring on the telephone wires. This covers the part of the characteristic from zero volts to the rated maximum repetitive off-state voltage, V_{DRM}. Also, after an overvoltage that causes the protector to switch, switch off must occur to restore normal operation. Switch off occurs at the low current termination point of the on-state region called the holding current, I_H.

Two off-state current conditions are normally specified, one for standby and the other at the system normal maximum voltage level. In POTS (Plain Old

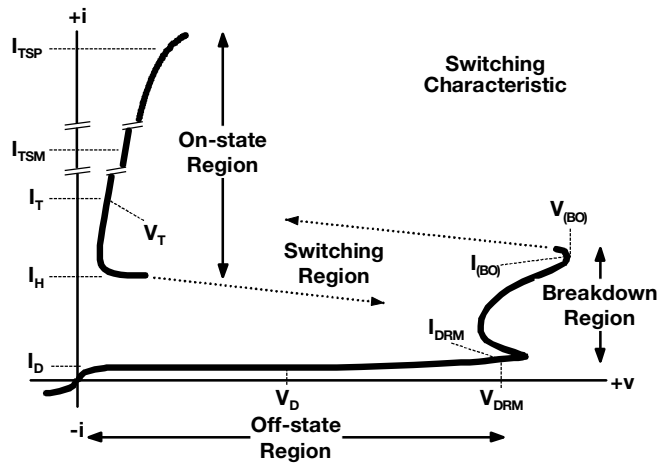


Figure 12. Switching Characteristic Regions and Parameters

Telephone Service) lines, in standby, the line normally has a battery voltage applied. This battery voltage is typically about -50 V. At standby, it is important that the protector draws little current. To ensure this, a d.c. off-state voltage, V_D, equal to the battery voltage, is applied and the resulting off-state current, I_D, measured. Increases in ambient temperature increase I_D, so it is important to specify I_D to be measured at the highest expected ambient temperature. As the standby is the normal line condition, durability testing often uses this as the electrical bias on the device.

The second off-state test comprehends the maximum line voltage resulting from the system signal or testing or ringing conditions. Under the normal system maximum voltage condition, the protector should not clamp and distort the voltage. To ensure this, the protector's repetitive off-state voltage rating, V_{DRM}, is set to be equal or greater than the maximum system voltage. For the rating verification test, the voltage is ramped up across the device and the repetitive off-state current, I_{DRM}, is measured when the voltage reaches V_{DRM}. The low-current breakdown voltage region is temperature dependent at a rate of about 0.13 %/°C. Characteristic curves of this are often included in TISP® data sheets. This means that any clipping will be most severe at the lowest ambient temperature. Therefore, V_{DRM} should be measured at the lowest expected equipment ambient temperature, or at 25 °C with an appropriate increase in the V_{DRM} value.

Device junction capacitance decreases with increasing applied voltage. Capacitance is measured with a specified d.c. and the a.c. bias voltage levels, e.g. -5 V and 1 V r.m.s. The a.c. voltage adds and subtracts to the d.c. voltage and at any moment the net voltage applied is the sum of the d.c. and instantaneous a.c. voltage values. The instantaneous capacitance value will be set by this voltage sum. Thus, as capacitance testing normally uses 1 V r.m.s a.c., the capacitance value measured will be an average value resulting from an applied voltage that varies ±1.4 V on a mean (d.c.) value. When the d.c. voltage bias is much greater than the a.c. voltage bias, the variation in capacitance caused by the a.c. is negligible. The capacitance is not frequency sensitive, but both circuit and package inductance can resonate with the capacitance and this is a more important frequency consideration. The capacitance measurement conditions should reflect the expected d.c. voltage bias, V_D, and, if possible, the appropriate a.c. voltage signal level, V_d. TISP® data sheets contain capacitance values for several d.c. voltage bias levels and often have graphs of capacitance versus voltage.

When the protector switches into the on-state, it diverts the line d.c. feed current as well as the current resulting from the overvoltage. After the overvoltage current stops, the protector must switch off to restore normal operation (transparency). This means that the protector's switch off current, called holding current, I_H, must be higher than the line d.c. feed; otherwise the protector would stay on. As the value of I_H decreases with increasing temperature, I_H should be specified to be equal to or higher than the line d.c. feed at the highest expected ambient temperature. Most TISP® data sheets contain a graph of I_H versus temperature. The holding current value is determined by switching the protector on to a specified on-state current level, I_T, then ramping down the current until the protector switches off. The current level where switch off occurs is the device I_H.

Protection

There are three areas concerned with the protection function; protection voltage, rated current capability and safety performance.

The protector must limit the voltage to a level that the following circuits can withstand (Figure 3) under both a.c. and impulse conditions. In the breakdown region, the peak voltage developed is called the breakover voltage, $V_{(BO)}$, and the current at this point is $I_{(BO)}$, the breakover current.

AC conditions can range from a few cycles of high current, terminated by the operation of the overcurrent protection, to 900 s or more of low level current. To cover the a.c. condition, the TISP® $V_{(BO)}$ is normally measured with a voltage ramp of 250 V/ms and 750 V/ms and a source resistance of 300 Ω. Under a.c. conditions, the values of $V_{(BO)}$ and $I_{(BO)}$ are major factors in the breakdown region power loss. So, for a.c. conditions, both $V_{(BO)}$ and $I_{(BO)}$ are measured.

Under impulse conditions, $V_{(BO)}$ will strongly depend on the impulse di/dt in the breakdown region. (Note: this is the dual of Gas Discharge Tubes, GDTs, whose peak limiting voltage depends on dv/dt.) To cover the impulse condition, the TISP® $V_{(BO)}$ is normally measured at 20 A/µs. The unclamped voltage rise is 1000 V/µs from a source resistance of 50 Ω. Other impulse voltage alternatives are: $V_{(BO)}$ for a specific impulse wave shape (e.g. 2/10), the limiting voltage-time envelope for a specific impulse wave shape (TISPPBL3) or a graph of $V_{(BO)}$ versus di/dt.

Standard	Peak Voltage Setting V	Voltage Waveform	Peak Short Circuit Current A	Current Waveform
GR-1089-CORE (February 1999)	2500	2/10	2 x 500	2/10
	1000	10/1000	2 x 100	10/1000
FCC Part 68 (March 1998)	1500	10/160	200	10/160
	800	10/560	100	10/560
	1000 1500	9/720 †	25 37.5	5/320 †
ITU-T covering: K.20 (02/2000) K.45 (02/2000) K.21 (10/2000)	1000 1500 4000 6000	10/700	25 37.5 100 150	5/310

† FCC Part 68 terminology for the waveforms produced by the ITU-T recommendation K.21 10/700 impulse generator

Table 1.

As with $V_{(BO)}$, the current ratings need to be specified for a.c. and impulse conditions. AC ratings such as peak non-repetitive on-state current, I_{TSM}, for given times, are usually given as spot values in the data sheet rating table. TISP® data sheets will often show a graph of I_{TSM} versus time, as well. As the current through the protector is quasi-sinusoidal, the current is expressed as a peak value rather than an r.m.s. value. Overcurrent protector operating time is expressed for d.c. or r.m.s current values. The overcurrent and overvoltage protectors are coordinated if, at a given current level, the overcurrent protector operates before the overvoltage protector reaches its time limit. To make this comparison, the respective current values must be converted to a common format, either peak or r.m.s.

To cover international and national standards and recommendations, the peak impulse non-repetitive on-state current, I_{TSP}, rating must be given for a wide range of waveshape designations. Common impulse waveshape designations are shown in Table 1 below.

Impulse current ratings vary with temperature. Designers should check that the I_{TSP} rating is adequate for the expected temperature range. Depending on the TISP® Series, the I_{TSP} temperature range can be -40 °C to +85 °C or 0 °C to +70 °C, or expressed as a graph of I_{TSP} versus temperature.

Sometimes there will be a series resistance before the TISP® device which will reduce the impulse current levels. The reduction in impulse level may allow the use of a lower current rated protector.

The on-state voltage, V_T, at a specified on-state current, I_T, is often quoted for historical thyristor reasons. In practice, a V_T value is not particularly useful as it is only a given current power loss, which is already comprehended in the I_{TSM} and I_{TSP} ratings.

Safety standards often specify tests that will cause protector failure to monitor the resultant fault mode and

check that there are no safety hazards. This type of requirement is covered in the TISP4350L3BJ data sheet.

Test Description	Conditions	Duration	LTPD %	Standard	Method
High Temperature Reverse Bias	150 °C, 80 % RV	1000 h	3	MIL STD 750	1048
Biased Humidity	85 °C, 85 % RH, -50 V	1000 h	3	JEDEC STD 22	A101
Temperature Cycle	-85 °C To +150 °C	200 cycles	3	MIL STD 883	1010
Solder heat	260 °C	10 s	10	MIL STD 750	2031
Solvent Resistance	3 Solvents		20	MIL STD 883	2015
Solderability	245 °C, After 8 h Steam Age	5 s	7	MIL STD 883	2003

Table 2.

Durability

Operated with their rated a.c. and impulse values, TISP® devices have an extremely long operating life, e.g. 10^5 impulses. Environmental and assembly reliability are covered by the TISP® qualification procedures. All TISP® devices are qualified in accordance with the standards listed in Table 2 prior to production release. Accelerated stress tests are chosen to ensure new products will meet the reliability requirements of the telecom industry. Each quarter, samples representative of the function and technology of the TISP® range are monitored to ensure that reliability remains satisfactory over the production life of the product.

Additional TISP® Electrical Requirements and Terms

Conducting unidirectional protectors will have a diode characteristic in one voltage polarity - Figure 13. The diode forward voltage, V_F, at a specified forward current, I_F, is the limiting voltage for the protected circuit. To cover a.c. conditions, the V_F should be given at a series of I_F values or as a graph. Under impulse conditions, the diode conduction may be delayed, leading to a short term increase in conduction voltage called forward recovery voltage, V_{FRM}. Like impulse $V_{(BO)}$, V_{FRM} is a function of impulse initial di/dt and can be given for a specific impulse wave shape (i.e. 2/10) or a graph of V_{FRM} versus di/dt.

Although the diode has its own rating letter symbols, the thyristor ones are often substituted; I_{TSM} for peak non-repetitive forward current, I_{FSM} and I_{TSP} for peak impulse non-repetitive forward current, I_{FSP}.

Fixed Voltage TISP® Function Range

Table 3 lists the current range of fixed voltage devices. Two terminal devices are basic building blocks. These are the bidirectional TISP4xxx and the unidirectional conducting TISP5xxx Series (unidirectional blocking devices are also made for specific customers needs). A single device can be used to limit the voltage between wires or between several points if placed on the d.c. output of a diode bridge. Two devices can be used on a 2-wire telecom line to limit the conductor voltage to protective ground by connecting each device between a wire and ground. There are three protection points involved here; the two wires and ground. This protector arrangement gives two modes of protection, which will be where the protector is directly connected between each wire and ground. The voltage between the wires will be limited by operation of the two protectors in series and this will be higher than the

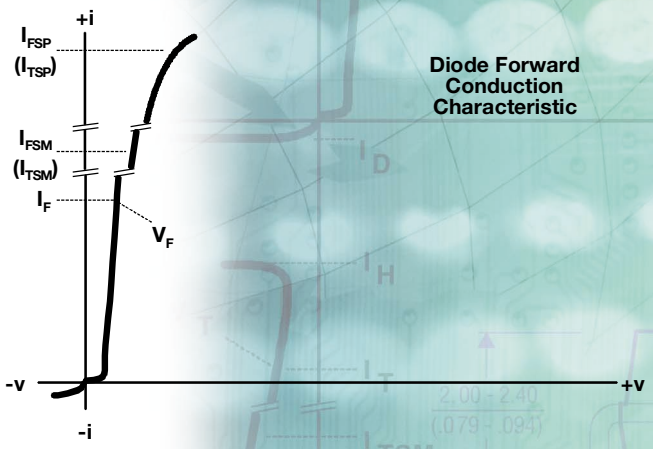


Figure 13. Diode Characteristic and Parameters

limited voltages to ground. Connecting a third protector between the wires gives direct inter-wire voltage limiting and 3 modes of protection. Modes of protection are classified by the protector being directly connected between those terminals. Indirect routes, via other terminals, do not count.

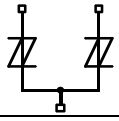
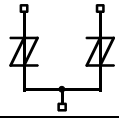
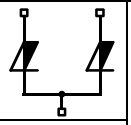
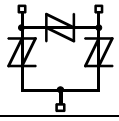
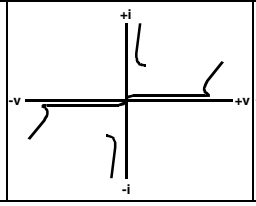
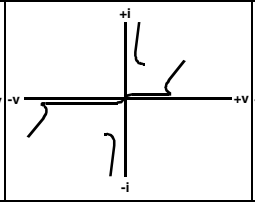
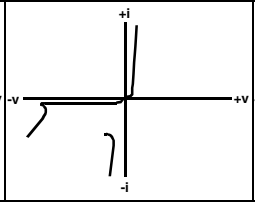
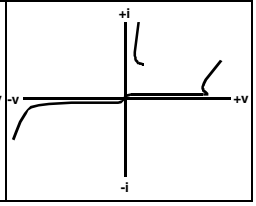
Fixed Voltage TISP® Configurations						
Protection Points	Protection Modes	Integrated Protection Elements	Class			
			Bidirectional		Unidirectional	
			Symmetrical	Asymmetrical	Conducting	Blocking
2	1	1	TISP4xxx Series 		TISP5xxx Series 	Custom 
3	2	2	TISP3xxx Series 	Custom 	TISP1xxx Series 	
3	3	3	TISP7xxx Series 			
Protection Mode Terminal Pair VI Characteristic						

Table 3.

The original design of the TISP® device allowed the integration of multiple protective elements. The current product range integrates the 3-point protection function into a single silicon chip. The TISP3xxx and TISP1xxx Series have 2 mode protection. As a standard, the TISP3xxx has a symmetrical protection characteristic in both voltage polarities. Special variants can be made where the protection characteristic is asymmetrical.

The TISP7xxx Series is a 3-point protector with 3 mode protection. As a standard, the TISP7xxx has the same protection voltage between any terminal pair; that is each wire to ground and wire to wire. Special variants can be made where the wire to wire protection voltage is lower than the wire to ground voltage.

Graphical symbols used in this table represent the protective characteristic measured at the device terminals. For ease of integration or to meet certain performance requirements, the integrated protection elements might not be of the form shown in the graphical symbol. This is similar to the graphical symbol of a triangle used to represent an operational amplifier which actually consists of many transistors and other components. The final row of the table is a graphical reminder of the VI characteristic of the various protection classes.

Gated TISP® Protection Function

These TISP® devices have a gate electrode, G, which controls the TISP® switching threshold. When the voltage between the gate and its adjacent electrode reaches a threshold value, TISP® current conduction is initiated. Further voltage increase causes the TISP® device to switch.

There are two main applications for gated TISP® devices: protection voltage level setting by using an external voltage reference, and current triggering by the overstress current. Normally, TISP® devices work as overvoltage protectors by diverting current. In the current triggered mode, the gated TISP® device still diverts current, but the current diverted was previously taken by the protected load.

Gated TISP® Structure

Gates are formed by making connections to the intermediate silicon layers of a fixed voltage TISP®

device. Gates are named by the type of silicon layer they connect to: N-gate or P-gate. Figure 14 is the fixed voltage structure of Figure 7 with gates added. The p layer, adjacent to the cathode n+ layer, has a P-gate electrode connection. The thyristor can be switched on by a positive voltage applied to the P-gate-cathode electrode pair.

The n- layer, adjacent to the anode p layer, has an additional n+ diffusion for the N-gate electrode contact. The thyristor can be switched on by a negative voltage applied to the N-gate-anode electrode pair.

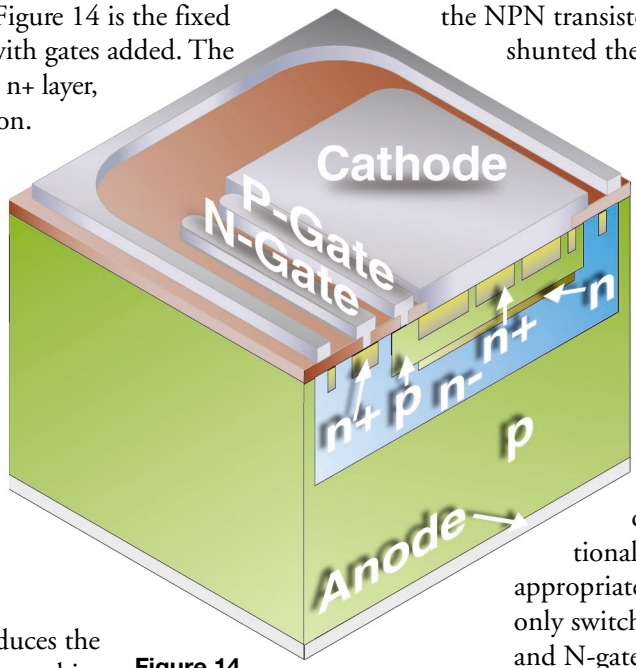


Figure 14.
Gated Protector Cross Section

Section (a) of Figure 15 reproduces the lumped equivalent circuit and graphic symbol of Figure 8. The gates of Figure 14 connect to the bases of the NPN, TR1, and PNP, TR2, transistors in the lumped equivalent circuit. The P-gate connection to the base of the NPN transistor creates a P-gate SCR (Silicon Controlled Rectifier) or simply an SCR, as this is the most common form of SCR ((b) of Figure 15). The N-gate connection to the base of the PNP transistor creates an N-gate SCR ((c) of Figure 15). In the N-gate SCR lumped equivalent circuit, shunt resistor RH, which sets the thyristor holding current, has been moved from the NPN transistor base-emitter to the PNP transistor base-emitter. If RH had been left across the NPN transistor base-emitter, it would have shunted the reverse blocking characteristic.

Current Triggered Operation

In the normal circuit-current triggered mode, the voltage measurement reference terminal is the non-adjacent electrode to the gate: anode for the P-gate and cathode for the N-gate. The ground connected reference terminal passes the diverted current to ground. The gated devices of Figure 15 are unidirectional and will only switch in the appropriate voltage polarity. P-gate SCRs only switch in the negative voltage polarity and N-gate SCRs switch in the positive voltage polarity. This P-gate and N-gate SCR pair is called a complementary pair as their terminal current and voltage polarities are opposites.

Figure 16 shows the appropriate bias conditions for the complimentary SCR types. The P-gate SCR is operated with the anode grounded, the cathode connected to the incoming wire and the gate connected to the protected load. At a negative voltage, -v, a current -i is drawn from the protected load. As the current flows though the parallel combination of the

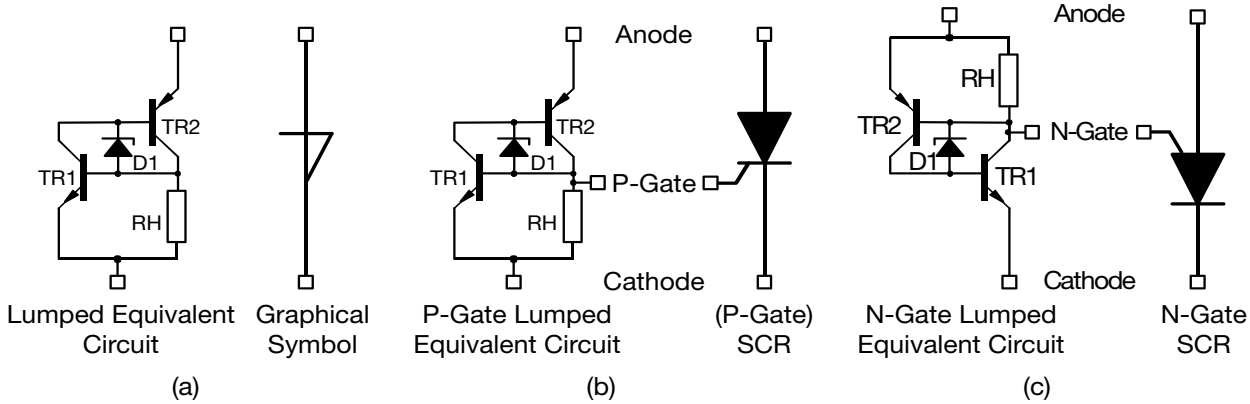


Figure 15.
Fixed Voltage, P-gate and N-gate SCR Circuits and Symbols

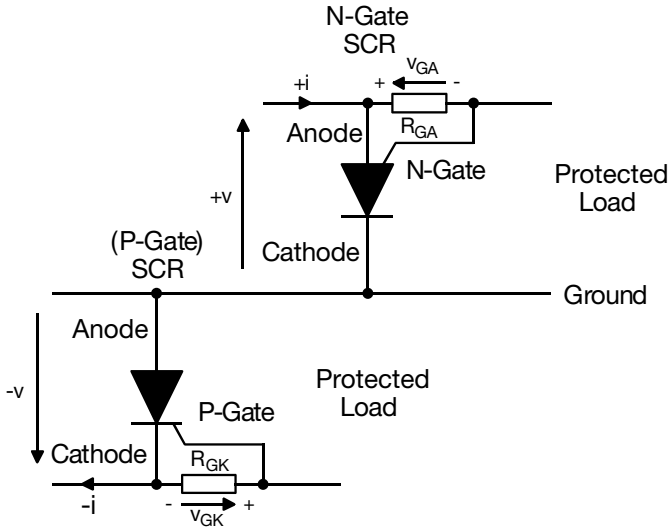


Figure 16. Current-Triggered SCR Bias Conditions

SCR gate-cathode resistance and the resistor R_{GK}, a voltage, V_{GK}, is developed that is positive with respect to the SCR cathode. To switch the SCR into the on state, the value of V_{GK} must reach the gate triggering voltage, V_{GT}, which is about 700 mV. The circuit current, i_S, to cause switching depends on the SCR triggering current, I_{GT}, and the value of R_{GK}. If I_{GT} was 25 mA and the required circuit current to trigger was 200 mA, the value of R_{GK} becomes 700/(200 - 25) = 4 Ω. Thus, when the incoming negative overvoltage draws 200 mA from the protected load, the SCR will switch on, diverting the current caused by the overvoltage from the protected load to ground.

The operation of the N-gate SCR in the positive polarity is the same as the P-gate SCR in the negative polarity. The complimentary description requires polarity reversal of the voltages and currents, plus the exchange of anode and cathode references.

A complimentary SCR pair is required to protect a single wire against positive and negative voltages, Figure 17. Referencing the composite protector electrodes is a problem as the P-gate SCR anode joins to the N-gate cathode and the P-gate SCR cathode joins to the N-gate anode. To solve this problem the electrodes are named MT1 and MT2. Electrode MT1 (Main Terminal 1) is the electrode connection that is adjacent to the gate and electrode MT2 is the non-adjacent electrode connection to the gate. In addition to complimentary SCRs, this bidirectional function is given by a device called a TRIAC (Triode for Ac Control), which is used in 50 Hz/60 Hz applications.

In the current-triggered mode, the SCRs provide current limiting to the protected load. By incorporating a defined voltage breakdown region in the SCR structures, the SCRs will limit the maximum voltage to the load as well, by operating as fixed voltage protectors. When operating in the fixed voltage mode, the current from the protected load is not needed to cause switching.

Voltage Reference (Tracking) Operation

As in the current-triggered mode, the voltage measurement reference terminal is the non-adjacent electrode to the gate. For voltage tracking operation, the gate is connected to an external voltage reference which controls the working and protection voltage. A simplified circuit is shown in Figure 18.

In Figure 18, the P-gate SCR is operated with the anode grounded, the cathode connected to the incoming wire and the gate connected to a power supply which biases the gate at voltage $-V_G$. For the SCR to trigger and switch on, the negative voltage, -v, on the wire must be equal or greater than the sum of the gate bias, V_G, and the gate-cathode voltage for SCR triggering. The triggering voltage, V_{GT}, is about 0.7 V, so the protection voltage is ($-V_G$ -0.7). If V_G varies, the negative protection voltage will track the changes with an offset of -0.7 V. Similarly, the

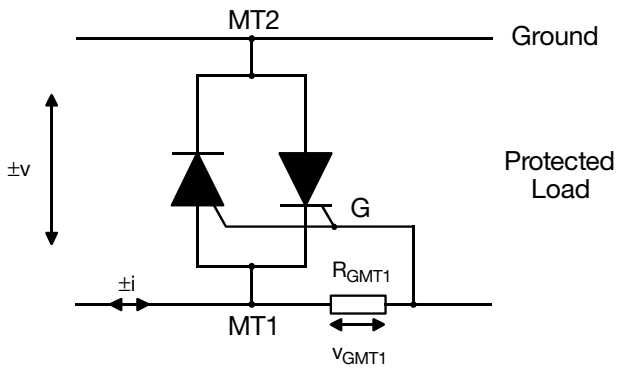


Figure 17. Bidirectional Current-Triggered Protection

protection voltage of the N-gate SCR will track the positive gate bias, $+V_G$, with an offset of 0.7 V. These voltage tracking protectors are sometimes called programmable protectors.

In practice, the gate bias voltage comes from the supply powering the SLIC (Subscriber Line Interface Circuit) used to drive the telephone line. This form of tracking protection ensures that the SLIC overvoltages are limited close to the power supply voltage. A fixed voltage protector cannot give the protection voltage precision of a tracking protector.

The simplified circuit of Figure 18 has two fundamental problems. One is that SCR input resistance, which can be in the region of 30 Ω, will create an excessive leakage current between the gate power supply and the wire. The second problem is when the SCR switches on, it will also try to pull the gate power supply voltage to ground as well as the wire voltage. Both these problems can be prevented by inserting a series gate diode block reverse gate current as shown in Figure 19.

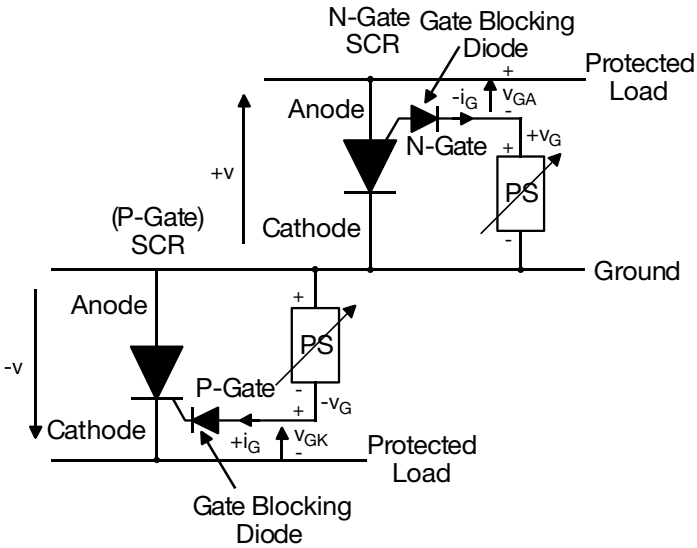


Figure 19. Use of Gate Diodes to Block Reverse Current

An IC based protection thyristor incorporating this blocking diode was proposed in 1986. By 1989, several parts were commercially available. This still left one problem, which was caused by the nature of the power supply. Typically, the power supply used

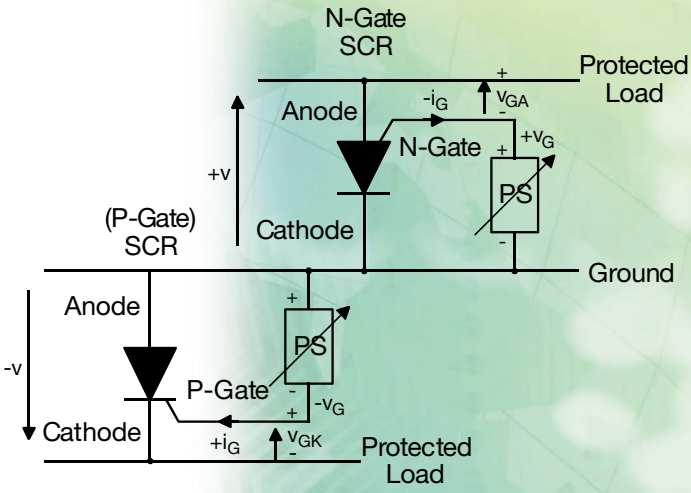


Figure 18. Simplified Voltage Tracking Protection Circuit

would be a switching mode. Switching mode power supplies that rectify and smooth pulses can only supply current in one direction. Unlike a battery, these switching mode power supplies cannot accept reverse current, i.e. they cannot be charged like a battery.

The problem this causes is shown in Figure 20. AC induction testing at low levels of V_{AC} gives a cathode currents, I_K, too low to cause switching of the SCR, Th1. The peak negative voltage is clamped just below the gate supply voltage of -50 V. A proportion of the cathode current appears as gate current, I_G. The reason for the gate current dipping in the middle of the negative a.c. cycle is SCR regeneration, which reduces the gate current value needed to support the cathode current. As the gate current does not fall to zero, the SCR never regenerates sufficiently to switch on. The gate current peaks at 80 mA and averages out to 21 mA. Unless the SLIC is drawing at least 21 mA via diode D2, the net current of the negative voltage power supply will be positive, i.e. a proportion of the gate current will be charging the power supply. Once the voltage starts to lower, most switching mode power supply loops will stop producing charging pulses. This reverse biases the rectifier diode D1, leaving the gate current to charge the voltage lower and lower. This situation often results in the SLIC failing due to overvoltage.

The SLIC illustrated does not need to produce positive voltages. The overvoltage protection in the

positive polarity is given by diode D4, which clips the voltage just above ground. Gate current during diode conduction is zero.

Some solutions to this problem are shown in Figure 21. Figure 21 is a simplified form of the Figure 20 circuit. Two SCR variants are shown: one as in Figure 20 and the other with a transistor TR1 replacing the gate diode D3. The graph shows the average current produced by the two variants. The SCR average current peaks just before the SCR starts to switch. Higher levels of a.c. test voltage, V_{AC}, reduce the voltage clamping time of the SCR and the average gate current. Breakdown diode D5 is added to divert current when the gate current starts to charge the power supply. This diode is often sacrificial, overheating and going short circuit under adverse power induction conditions.

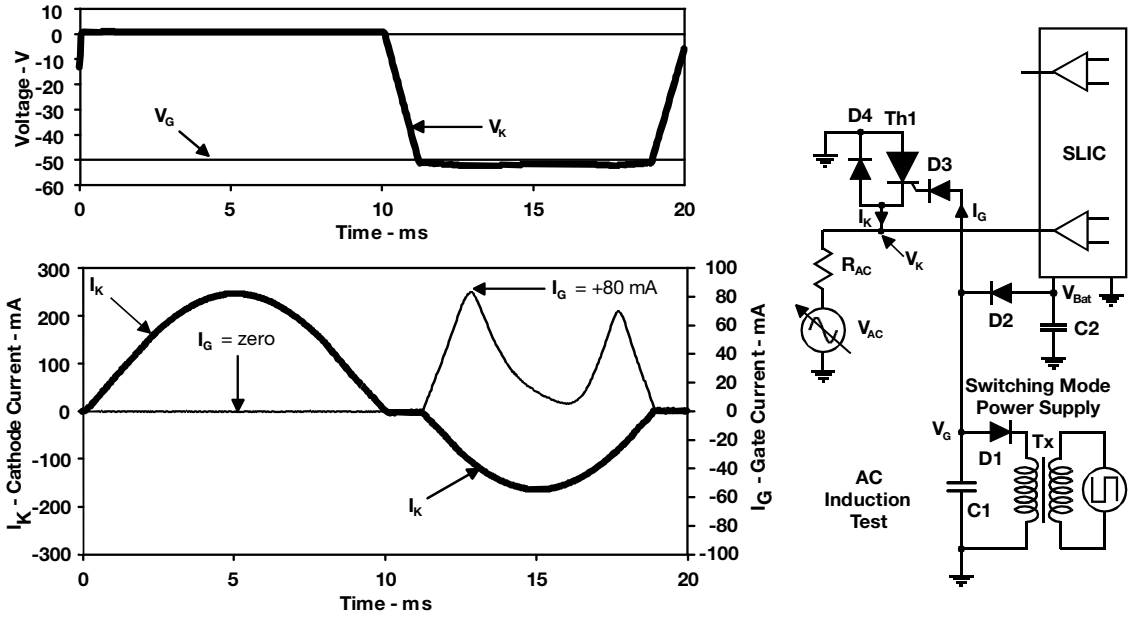


Figure 20. AC Induction Testing

The transistor buffered SCR shows an unexpected characteristic - the average gate current is negative, so always correctly loading the power supply. The gain of the transistor will reduce the average gate current during cathode current flow, but this will still be a positive value even though it is lower than the unbuffered SCR gate current. Figure 22 provides the answer; there is negative current flow during the diode D4 conduction. By careful integration, some of the diode current diverts to the transistor base causing a negative gate current flow during diode conduction. The peak positive gate current is 1.6 mA and the peak negative gate current is a larger -7 mA.

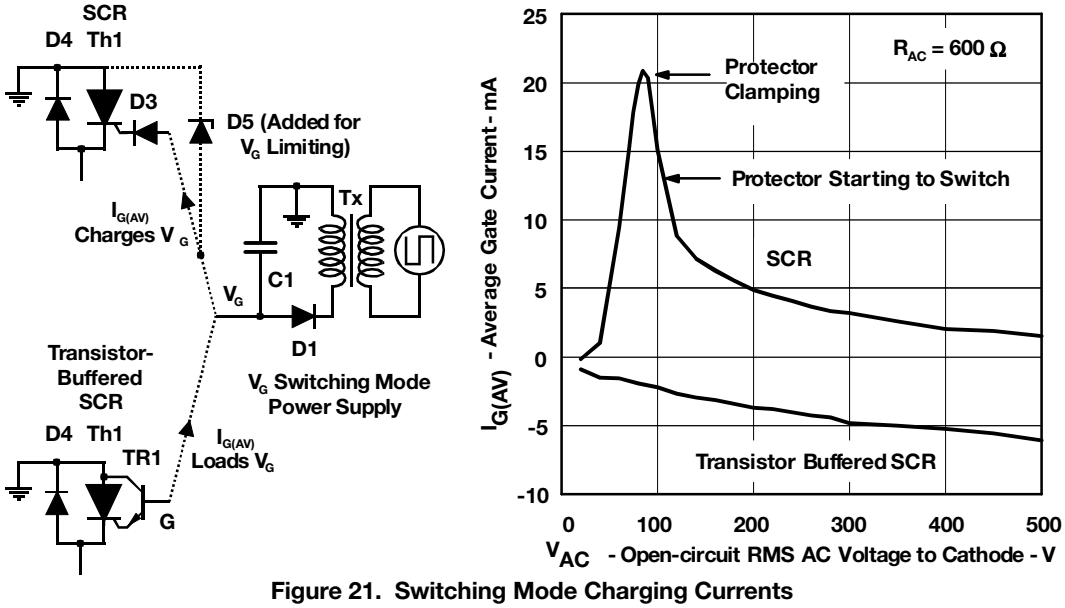


Figure 21. Switching Mode Charging Currents

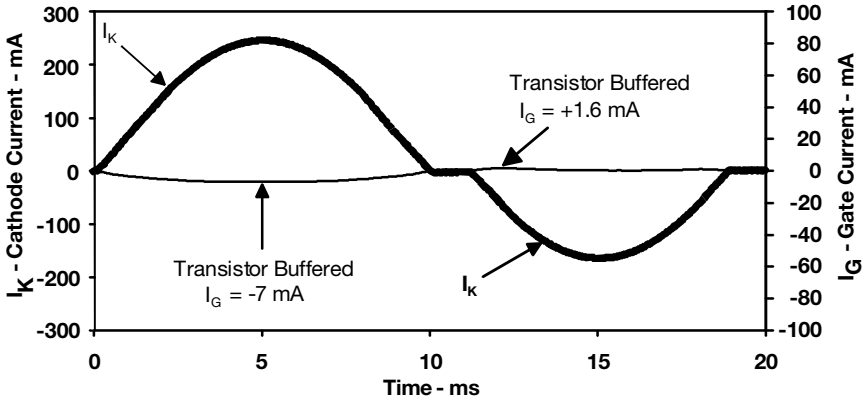


Figure 22. Transistor Buffered SCR Currents

Protectors like the TISP61089B are designed on this principle.

Transistor Buffered Thyristor Structure

Figure 23 shows how the NPN transistor is integrated with the P-gate SCR. The NPN transistor is formed from the starting silicon n- material and diffusion of p+ and an n- conversion. Low resistance contact areas for the collector and emitter electrodes are given by further n+ diffusion. A metal strap connects the transistor emitter to the SCR P-gate. This type of structure is used in the TISP8200M devices and a complimentary version for the TISP8201M devices (PNP transistor and an N-gate SCR).

Gated TISP® Function Range

Gated devices can be made in the same classes as fixed voltage devices: conducting unidirectional, blocking unidirectional, symmetrical bidirectional and asymmetrical bidirectional. Likewise, the protection modes can be single or multiple in a single package. The extra dimensions gated devices bring are P-gate, N-gate or both, plus buffered or unbuffered. Adding these gate options to the fixed voltage classes and modes of Table 3 would make a complex table. Table 4 on the following page is a subset showing the catalog parts currently offered by Bourns.

The current product range integrates several 3-point protection functions into a single silicon chip. The TISP6xxxx Series, TISPPBL3, TISP8200M and TISP8201M have 2 mode protection. All are transistor buffered to reduce triggering current. The TISP6xxxx Series and TISPPBL3 are conducting unidirectional protectors intended for protecting negative battery voltage SLICs. The TISP8200M and TISP8201M are used as a pair to protect ringing SLICs which have plus and minus battery supplies.

The TISP6NTP2x series are 5-point protectors with 4 modes of protection. These devices integrate 4 conducting unidirectional protectors in a single package.

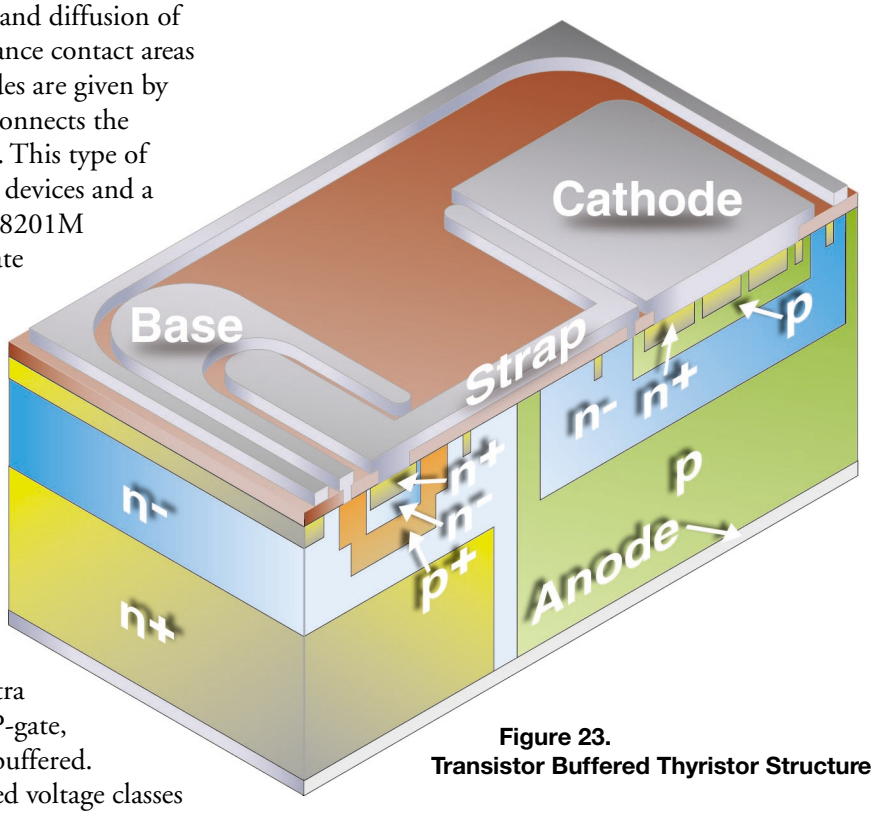


Figure 23.
Transistor Buffered Thyristor Structure

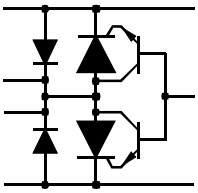
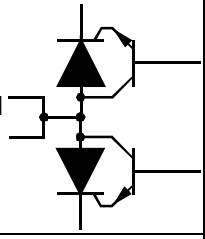
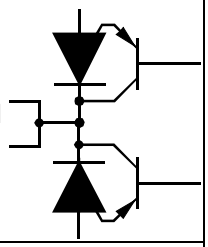
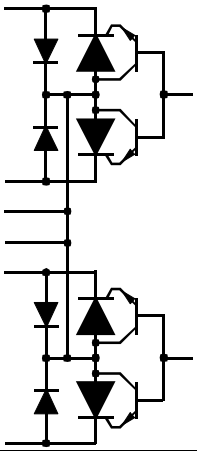
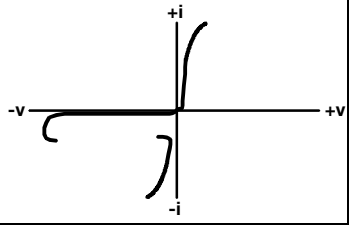
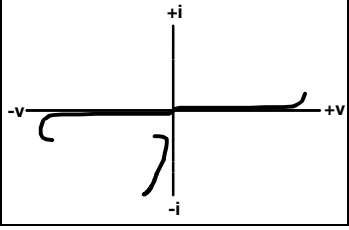
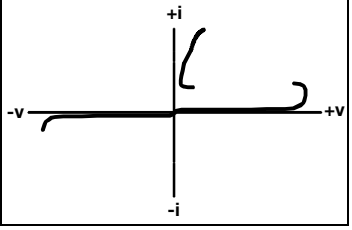
Gated TISP® Configurations					
Protection			Class - Unidirectional		
Points	Modes	Integrated Elements	Conducting	Blocking	
			Buffered P-gate	Buffered P-gate	Buffered N-gate
3	2	2	TISP61xxx Series TISPPBL3 	TISP8200M 	TISP8201M 
5	4	4	TISP6NTP2x Series 		
Protection Mode Terminal Pair VI Characteristic					

Table 4.

TISP® Packaging

When the TISP® device was first introduced in 1982, it used the standard TO-220AB power device package. This package, together with the smaller SOT82, was intended to be secured to a heatsink to allow high dissipation. Generally, the dissipation of a TISP® device does not require the use of a heatsink. This led to the introduction of various TISP® products in smaller, lower height through-hole mounting packages in the 1987 to 1998 period. Recognizing the trend to surface mount technology, in 1993 TISP® devices were introduced in 8-pin small outline packages, D008, and followed in 1997 by the 2-pin DO-214, SMB package. This path of migrating from power device packaging to smaller size through-hole package and the introduction of surface mount technology is shown in Figure 24.

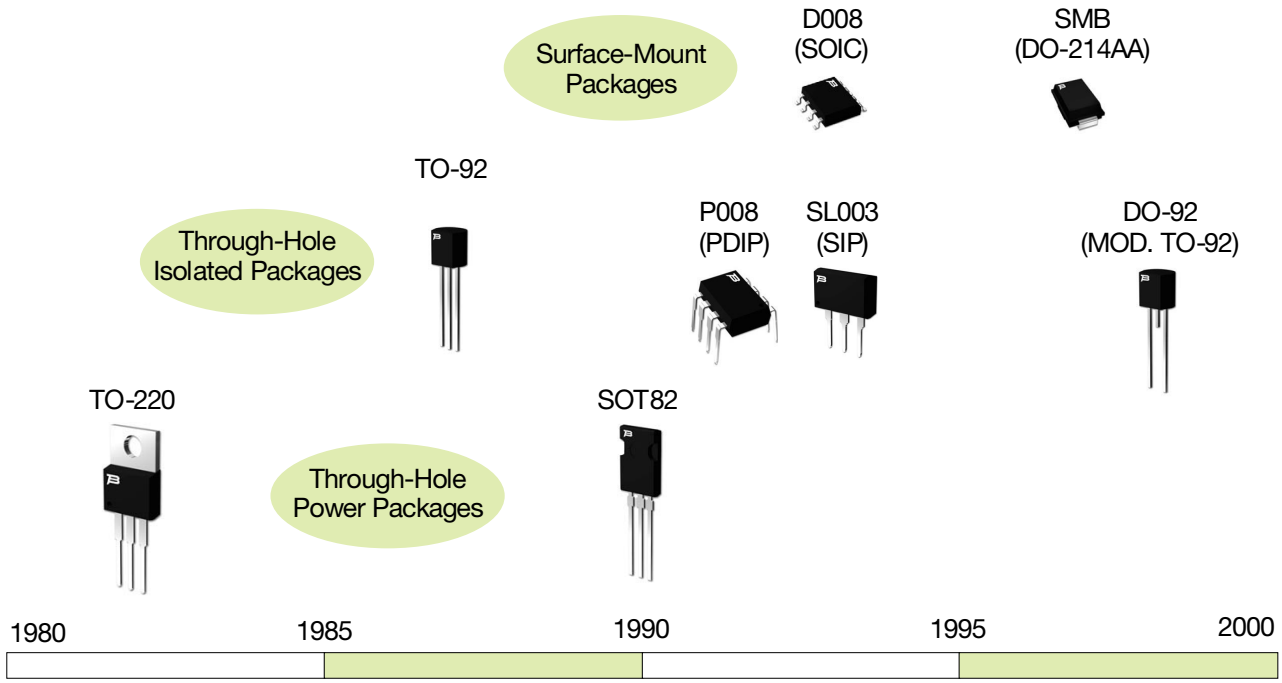


Figure 24. Package Introductions

Applications Information

TISP® data sheets are comprehensive and contain applications information relevant to that device. The following table lists some of the topics found in TISP® series data sheets.

Area	Topic	TISP® Data Sheet
Circuits	BOD replacement	’3700F3
	Diode bridge multi-point protection	’5xxxH3BJ
	LCAS (Line Card Access Switch)	’4125/’219H3BJ
	Low capacitance 3-point protection	’5xxxH3BJ
	SLICs - Ericsson	’PBL3
	SLICs - Ringing, negative supply	’61089B
	SLICs - Ringing, positive/negative supply	’8200M, ’8201M
	SLICs - Negative supply	’5xxxH3BJ
	System insulation protection	’3700F3, ’4700F3
	Transformer winding protection	’40xxL1BJ, ’40xxH1BJ
Standards	FCC Part 68	’4xxxL3BJ, ’4360H3BJ
	GR-1089-CORE	’61089B, ’6NTP2A
	IEC 61000-4-5	’6NTP2A
	IEEE Std 802.3	’3700F3
	ITU-T K.20, K.21	’6NTP2A
	UL 1950/60950, CSA 22.2 No.950	’4xxxL3BJ, ’3700F3

Area	Topic	TISP® Data Sheet
Systems	ADSL	’4360H3BJ
	HDSL	’40xxL1BJ, ’40xxH1BJ
	Home phone networking	’40xxL1BJ, ’40xxH1BJ
	ISDN - d.c. feed	’5xxxH3BJ, ’6NTP2B
	ISDN-S/U	’40xxL1BJ, ’40xxH1BJ
	LAN and MAN	’3700F3
	Pair Gain	’40xxL1BJ, ’40xxH1BJ
	xDSL	’6NTP2A
Equipment	ADSL MODEMs	’4360H3BJ
	POTS intra-building, - Cable MODEMs, - Router, - Set top boxes, WLL	’6NTP2A
Impulse Generators	GR-1089-CORE	’61089B
	IEC 61000-4-5 generator ITU-T generators	’7xxxF3

Table 5.