Title	Robust Protection and Excellent Signal Quality for Gigabit Ethernet Applications Using Transient Current Suppressor (TCS™) Technology
Authors	Andy Morrish and Len Stencel
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1 Introduction

Since the first electronic equipment was designed, engineers have had to deal with protecting their equipment against electrical surges, primarily Electrostatic Discharge (ESD) and lightning.

ESD is a common occurrence in everyday modern life. Many materials have *triboelectric* properties - that is, they allow charge to be transferred from that material to another by virtue of mechanical friction. Hence, someone walking across a carpet containing woolen fibers, in shoes with synthetic rubber soles, is very likely to accumulate electrostatic charge as they walk, with charges being transferred between the carpet and the shoes. As this charge transfer continues, the potential difference between the body and the surroundings increases, sometimes to tens of thousands of volts.

Per the ESD Association: "The age of electronics brought with it new problems associated with static electricity and electrostatic discharge. And, as electronic devices became faster and smaller, their sensitivity to ESD increased. Today, ESD impacts productivity and product reliability in virtually every aspect of today's electronics environment. Industry experts have estimated average product losses due to static to range [up to] 33 %. Others estimate the actual cost of ESD damage to the electronics industry as running into the billions of dollars annually."[1]

At the other end of the scale, static charge similarly accumulates on clouds. This electric field builds until the air breaks down, creating massive discharges of energy in the form of lightning. In contrast to the tens of thousands of volts accumulated by someone shuffling across a carpet, clouds can accumulate sufficient charge to reach billions of volts, with discharge currents reaching into the hundreds of thousands of amps, basically caused by the same triboelectric mechanism of charge transfer. This enormous discharge of energy results in localized potential differences across the surface of the earth, which can be very hazardous to electronic equipment interconnecting over even short distances.

As an indication of the level of damage caused by lightning, the New York based Insurance Information Institute has stated that the average cost per claim for lightning strikes in the United States increased 5.5 percent last year, driven by a rise in the number and value of consumer electronics. Lightning strikes cost insurers an average of $5,112 a claim in 2011, compared with $4,846 the previous year. "Plasma and high-definition television sets, home entertainment centers, multiple computer households, smart phones, gaming systems and other expensive devices -- which can all be destroyed by power surges -- continue to have a significant impact on claims losses," Loretta Worters, the institute's vice president, said in a recent statement.[2]

[1] http://www.esda.org/
[2] http://www.bloomberg.com/news/2012-06-21/high-def-tvs-means-lightning-strikes-cost-5-112-a-claim.html

Modern electronics, in the quest for ever higher speed and lower costs, use increasingly denser IC technologies, whose sensitivity to surges creates an increasingly difficult challenge for designers of electronic equipment.

Equipment interfaces can be exposed to a wide range of discharge events up to and including surges caused by lightning. Even with ESD-immune optical fibers transmitting data long distances, connection from the optical-electrical interface equipment to offices and residential buildings is still primarily through external conventional electrical cabling, exposing this equipment to high energy electrical surges.

As technology advances, older circuit protection solutions for prevention of high energy surge damage have become less effective. This white paper examines how the new Bourns® Transient Current Suppressor (TCS™) device, provides a high performance and cost effective solution to the transient electrical surge problems that continue to challenge modern technologies. After discussing the TCS™ device, we will apply it to a Gigabit Ethernet (GbE) application and present the test results when the design is subjected to various surge waveforms.

2 Limitations of a Transient Voltage Suppressor

2.1 Basic Operation of a Voltage Limiting Device

Electronic protection devices have been developed to absorb ESD energy at the interface, and one of the most commonly used devices is a Transient Voltage Suppressor (TVS) diode. The basic operation of a TVS diode is very simple (see figure 1). Ideally, it appears as high impedance in the normal range of the signal working voltage that passes over the line. Only when the surge at the interface exceeds a preset limit does the TVS diode become conductive, abruptly limiting the voltage from rising above this level.

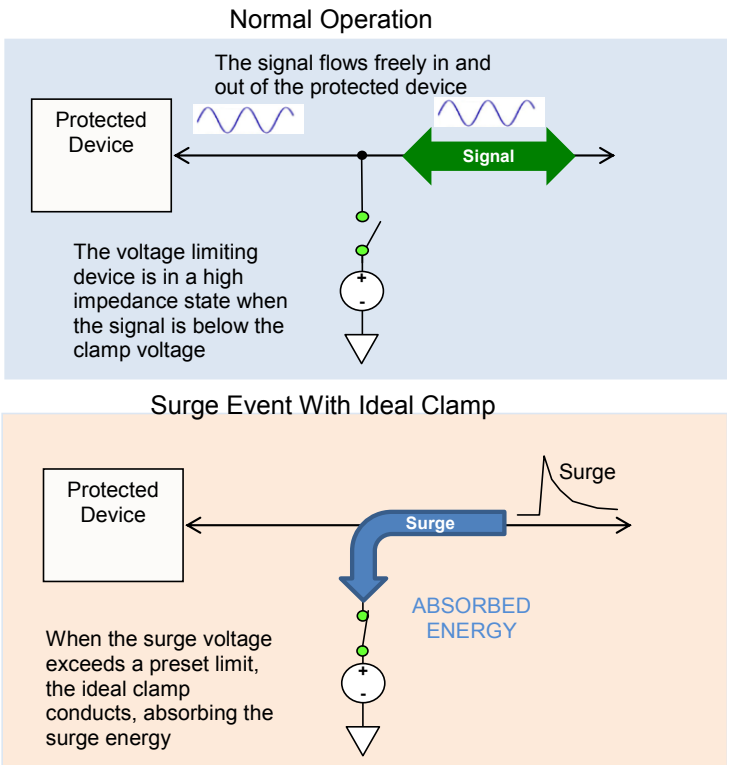


Figure 1. Basic Operation of an Ideal Voltage Limiting Device

The ideal TVS diode thus has a "brick wall" clamping electrical characteristic, as shown in figure 2, whereby the device causes no interference to the normal signal, yet prevents the voltage at the interface from ever going beyond a level that may be dangerous to the equipment.

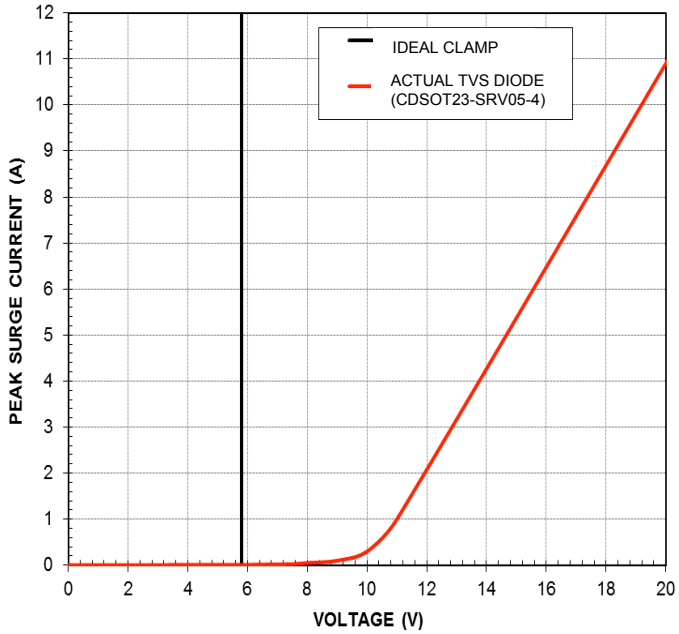


Figure 2. Comparison between an Ideal 5 V TVS Diode Characteristic (Black Line) and an Actual TVS Diode (Model CDSOT23-SRV05-4) (Red Line)

In practice, a TVS diode supports current flow in the form of avalanche, Zener or punch-through breakdown, depending upon the construction of the device. We immediately begin to see divergence from the abruptly vertical characteristic of the ideal clamping device when we compare it to a typical semiconductor TVS diode. The real TVS diode appears highly resistant as the voltage increases, but near the breakdown voltage of the junction, a finite amount of "leakage" current begins to flow. The larger the junction, the higher the amount of leakage, which can be very troublesome as this current can have a significant impact on the operation of the circuit, particularly at higher temperatures.

Secondly, the actual clamping characteristic is much softer than the abrupt vertical characteristic of the ideal clamp. Instead, as the clamping voltage is reached, the current begins to increase gradually, rather than with an abrupt right angled characteristic. In order that the onset of clamping does not interfere with the signal, the clamping voltage must make allowances for this soft transition into clamping behavior and the onset of clamping must be set relatively high compared to the ideal characteristic.

As the current level increases still further, a distinct gradient is seen in the voltage increase, caused by the significant internal resistance of the TVS diode. As ESD devices may conduct tens or even hundreds of amps for short durations, the actual peak voltage that may be seen across the device, and therefore across the line, will be significantly higher than the onset of breakdown. The internal resistance is inversely proportional to the junction area, and so achieving acceptably low clamping voltage at high levels of current may require a very large junction, which greatly impacts capacitance, cost and package size.

It becomes apparent that simply connecting a TVS diode between an interface and ground is ineffective in protecting the device driving that interface. The device will see the peak voltage developed across the TVS diode with a characteristic such as in figure 2. The voltage may reach 20 V during a discharge of 11 A, which is far beyond the capability of many low voltage technologies. Instead of effectively shielding the interface device from the surge, the TVS diode simply diverts a portion of the energy away, as shown in figure 3, still leaving the device exposed to high voltages and currents. This remaining energy seen by the protected device is often termed “let-through energy”.

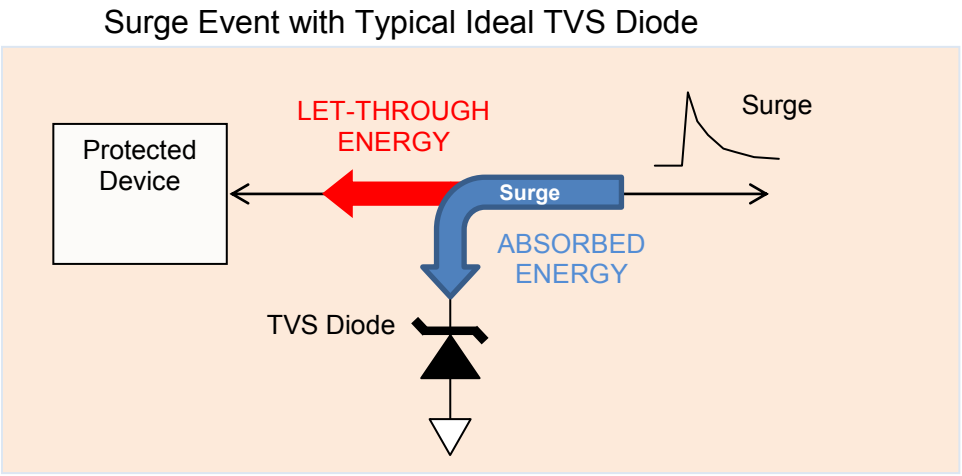


Figure 3. The Protected Device Experiences the Same High Voltage Transient as the TVS Diode

The potentially high level of let-through energy under surge conditions can be a major problem when using conventional TVS diodes for the protection of sensitive electronics in harsh environments.

2.2 Impact of TVS Capacitance on Signal Integrity

As data rates and transmission distances increase, a further consideration is the high frequency characteristics of the surge protection device during normal line use. High capacitance can cause unacceptable high frequency attenuation in the circuit, significantly limiting the capacity to drive high data rates. While linear capacitive effects can be compensated to some degree, a bigger problem is that semiconductor junction capacitance exhibits a high degree of nonlinearity when measured against applied voltage, as the depletion region width that sets the capacitance varies with voltage, shown in figure 4.

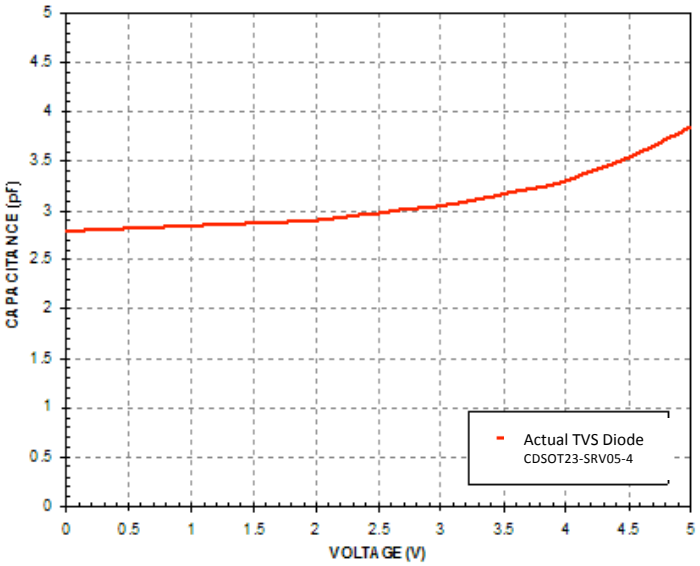


Figure 4. Typical Variation in TVS Capacitance vs. Voltage on Model CDSOT23-SRV05-4 Diode

This dynamic capacitance variation with signal voltage can result in unacceptable harmonic distortion of the waveform, causing spurious noise harmonics which drastically impact the achievable data rates over long distances in multi-tone systems such as VDSL.

Capacitance is another critical parameter that is proportional to the junction area; the larger the TVS diode, the higher the capacitance becomes.

2.3 Protection vs. Performance vs. Cost

It can readily be seen that a balancing act is required to choose the appropriate TVS diode; too small, and the junction will have inadequate clamping performance. If the device is too large, capacitive and leakage effects can cause major performance impacts, not to mention the larger devices typically will cost more to produce. TVS development has centered around optimizing the design of the diode to find a TVS performance that can clamp well without overly degrading the signal performance, and at the same, keeping within an affordable price, but this is a trade-off that is becoming more and more difficult to realize.

The lower voltage TVS diodes have become increasingly difficult and expensive to produce as interface driver device voltage systems such as Gigabit Ethernet have decreased, firstly from 5 V to 3.3 V, and then to 2.5 V and most likely in the future, even lower. For these lower voltage devices, more complex TVS diode designs must be used, as conventional diode junctions present increasingly high resistance and high leakage at low voltages. These TVS diodes have a structure resembling an open base transistor, which gives rise to a low voltage "punch-through" characteristic, rather than avalanche or Zener breakdown to control the clamp characteristics. This type of TVS diode often exhibits a degree of “fold-back”, whereby the clamping voltage drops as the clamp current initially begins to increase. A fold-back characteristic significantly helps to reduce the increase in clamping voltage at higher currents, but adds very significantly to the device complexity and cost compared to a simple P-N junction diode. Ironically, many system designers push for lower and lower voltage TVS diodes to follow the driver technology voltage, not realizing that under surge conditions the TVS voltage may rise to as much as 15-20 V, regardless of the rating!

3 The Transient Current Suppressor (TCS™) Device: A New Approach

The problems inherent in achieving ideal TVS characteristics, in combination with the growth in high-speed, low voltage applications that must withstand severe levels of lightning surge and ESD, invite an alternative approach. The basic limitations of the TVS diode stem from it being a single-stage protection device. Even the best voltage limiting device does not prevent current flow into the protected device, which often cannot withstand the levels of current that flow during the time when the clamping voltage is at its peak.

The Transient Current Suppressor (TCS™) device is a new approach that significantly improves the level of protection when used in series with the protected signal line, in a two-stage configuration together with a voltage limiting device. The actual characteristics of the TCS™ device are shown in detail in figure 5.

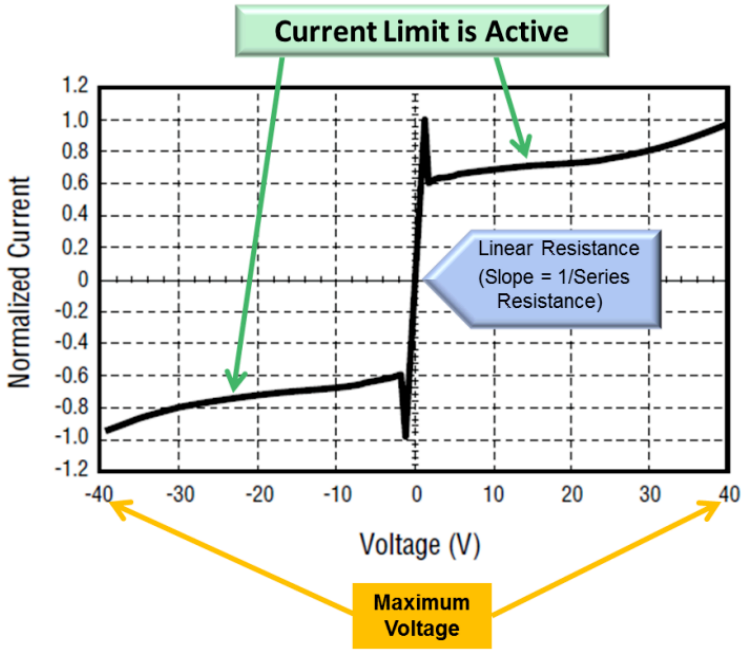


Figure 5. I-V Curve of a TCS™ Device

In normal operation, when normal signal current is low, the TCS™ device behaves as a low value resistor. Under surge conditions, when the current is driven above a certain limit, the TCS™ device transitions very rapidly into a current limiting state.

The TCS™ device configuration and circuit symbol are shown in figure 6.

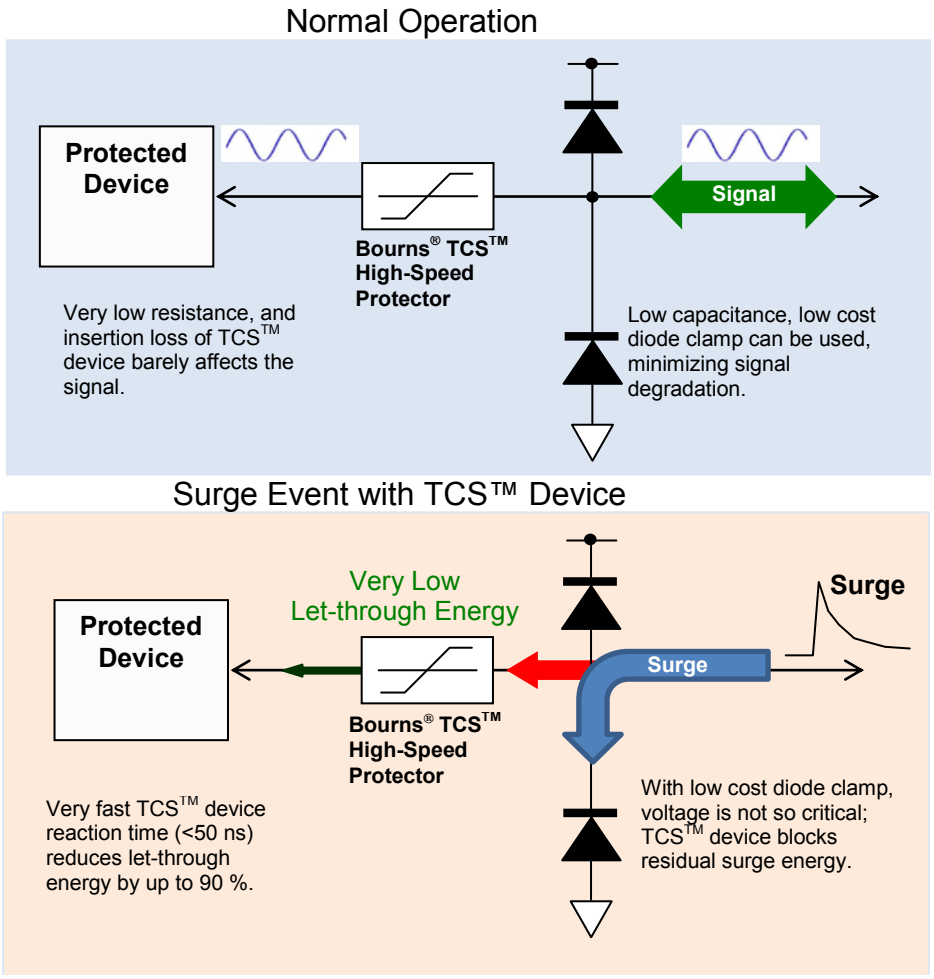


Figure 6. Implementation of a Transient Current Suppressor (TCS™) Device in a Circuit Protection Solution

The TCS™ device drastically reduces stress by adding a current limiting stage in series with the protected device to complement the characteristics of the voltage limiting device. When a surge occurs, the voltage at the interface increases, causing current to flow through the TCS™ device. As the current limit is reached, the TCS™ device prevents further increase in current within its rated limits by allowing the voltage across itself to increase, effectively presenting a very high resistance. As the current is limited to a constant level, the voltage at the protected device no longer rises, and stays within a safe level. On the other side of the TCS™ device, the voltage continues to rise until the activation voltage of the voltage clamping device is reached.

The first stage clamp voltage level no longer needs to be critically chosen to match the protected device, and its clamping characteristic may be much softer (resistive) than a single stage TVS diode would need to be. The voltage across the clamp voltage can continue to rise, with the maximum limitation now being that the differential voltage developed across the TCS™ device must stay within the 40 V breakdown voltage limit of the TCS™ device, a condition that is much easier to achieve, using most forms of voltage clamp.

As its name implies, the Transient Current Suppressor (TCS™) device is directly analogous to the TVS diode; whereas the TVS diode limits transient voltages, the TCS™ device limits transient currents. The simplified current and voltage diagrams in figure 7 show this comparison.

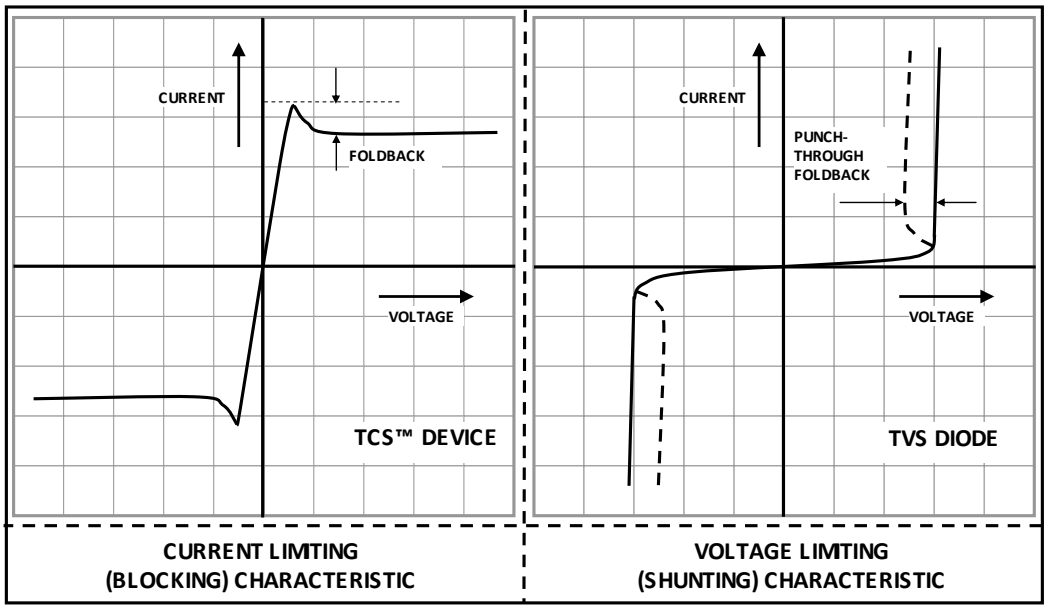


Figure 7. Complementary Characteristics of the TCS™ Device and TVS Diode

As can be seen from the characteristics, the TCS™ device, like the punch-through TVS diode, also exhibits a degree of fold-back, whereby the current drops approximately 30 % from its maximum value as the voltage increases further. This fold-back helps to minimize stress in the protected device and also improves transient power handling in the TCS™ device.

Several device options of resistance and current limit are available and can be chosen for optimal cost and performance in the application:

DEVICE	TYPICAL RESISTANCE (Ω)	TYPICAL CURRENT LIMIT (mA)
Dual Channel 40 V 250 mA	2.3	375
Dual Channel 40 V 500 mA	1.4	750
Dual Channel 40 V 750 mA	1	1125

The TCS™ device acts like a conventional linear low value resistor in series with the line, so there is no physical connection to ground for internal parasitic capacitance to occur. As with a resistor, the only significant capacitance is due to the capacitance between the body of the TCS™ device and its surroundings. For minimum capacitance, therefore, care should be taken during layout so that no electrical traces or planes are run under the packaged device. In particular, ground and voltage planes should have windows cut out directly beneath the device pads. When designed in this way, the capacitive loading effects of the TCS™ device are

negligible, even well up into the GHz region, making the TCS™ device ideal for enhancing the protection of very high-speed data buses.

The speed of the current limiting operation of the TCS™ device is ideal for protecting against standard lightning surge test waveforms (1.2/50 µs, 10/1000 µs etc.). The typical response time to achieve limiting operation is less than 50 ns. A very fast rising transition from zero current at rates greater than 5 kV/µs may cause the current to momentarily overshoot the nominal current limit by a small amount for a very short interval but the amount of additional let-through energy during this interval is negligible.

Dual channel TCS™ devices contain two well-matched series resistances in one package. For example, the TCS™ Dual Channel 40 V 750 mA device with a nominal resistance of 1 Ω is matched to just within 20 mΩ. Like resistors, TCS™ devices can be connected in parallel to give even lower resistance. The individual transient current suppressors in a dual TCS™ device can be paralleled to act as a single device with half the resistance and twice the current limit. If two matching parallel connected TCS™ devices are required, two dual devices can be used, with one transient current suppressor from each package connected in parallel to one transient current suppressor from the other package to retain good matching.

When used with even a basic voltage clamping device such as simple relatively high resistance signal diode clamps as in figure 6, the composite behavior of the TCS™ device in conjunction with a voltage clamping device closely matches that of the ideal "brick wall" clamping device, as shown in figure 8.

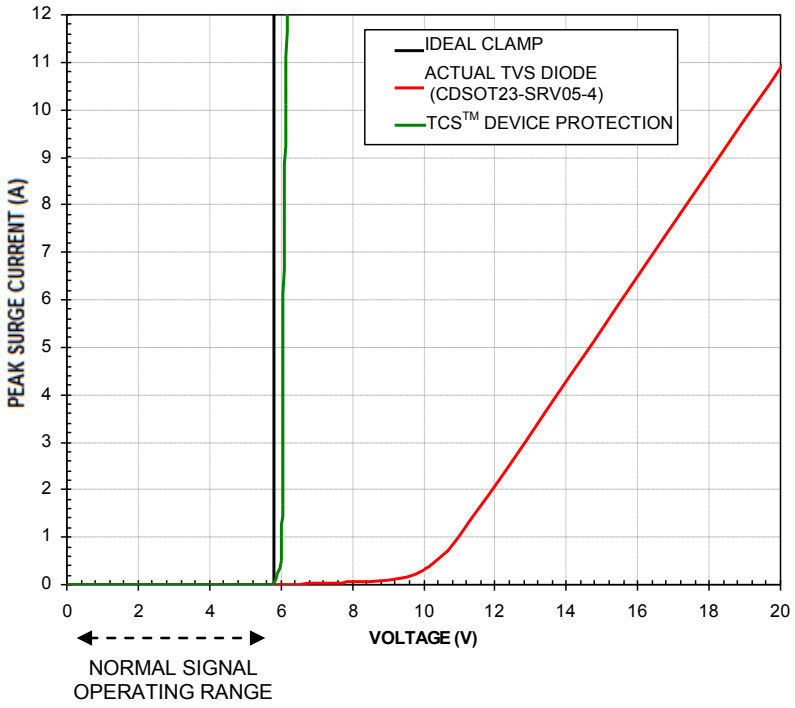


Figure 8. The TCS™ Device Model TCS-DL004-250-WH Behaves Like an Ideal Clamp Compared Against TVS Diode Model CDSOT23-SRV05-4

The table below shows how the TVS diode and TCS™ device have complementary characteristics:

TVS Diode	TCS™ Device
Limits voltage	Limits current
Parallel connection	Series connection
Shunting (shorting) protective action	Blocking (limiting) protective action
Very high resistance below max voltage	Very low resistance below max current
Very low resistance above max voltage	Very high resistance above max current
Adds parallel capacitance	Negligible parallel capacitance
Junction (bipolar) construction	Field-effect (MOS) construction

4 Characterization of Devices Used in a GbE Application

Before we evaluate the performance of the protection circuit for a GbE application, it would be beneficial to gather some information on the components that will be part of the system to get an idea how they will perform under surge conditions. Let's take a look at a few ethernet transformers, a TVS diode, a TCS™ device and some steering diodes. We will evaluate the components using the 1.2/50 µs, 8/20 µs combination wave called out in GR1089-CORE-ISSUE6 for port type 4, which is an intra-building port specification. For the differential (metallic) test, the standard (surge test number 12 in table 4-2) calls out using an external six ohm resistor in series with the fault source which has an internal output resistance of 2 ohms. The peak surge voltage for the test is 800 V, giving us a peak current of 100 A.

4.1 Ethernet Transformers

We will take a look at two Bourns® transformers (Models SM51589L and PT61020L) and one from another supplier. The initial test circuit for the transformer is shown in figure 9. The graph in figure 10a shows the primary and secondary current for these three ethernet transformers when tested with a 1.2/50 µs, 8/20 µs combination wave with a peak current of just over 100 A. The secondary winding is shorted for the test, representing the absolute maximum current that could be seen in the transformer secondary. The secondary peak current is reduced by about a factor of four. As important as the reduced peak current is, it is important to also note that the duration of the surge current is reduced to about 1-2 µs (at the 50 % point). This characteristic will greatly aid the protection of the ethernet physical layer (PHY).

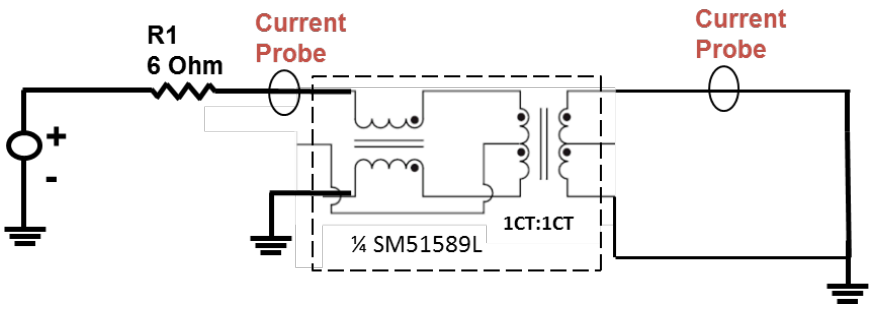


Figure 9. Initial Transformer Test Circuit.

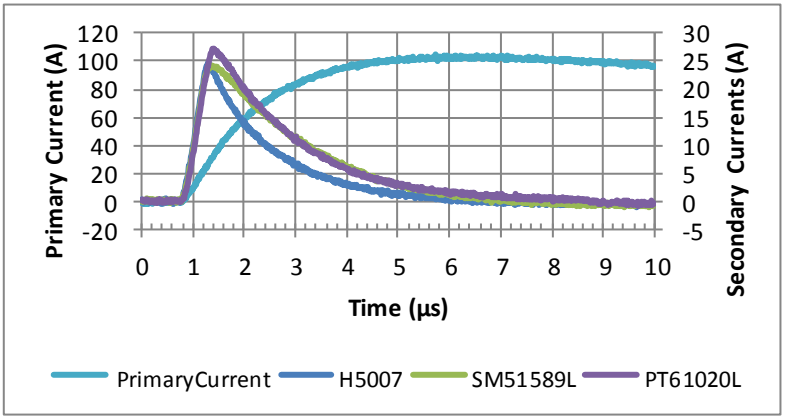


Figure 10a. Primary and Secondary Currents of Ethernet Transformers with Secondary Shorted

Now, if we use a 100 ohm termination in parallel with a 5 V TVS diode we get an even better picture of the peak current to expect in the application. The transformer secondary currents with this load on the secondary are shown in figure 10b. Note the reduction in the peak current as well as the shortened duration. For example, the peak secondary current for the Model SM51589L transformer was reduced to ~18 A from the 24 A that was measured with the secondary shorted. The width of the current pulse at the 50 % point was also reduced by about half.

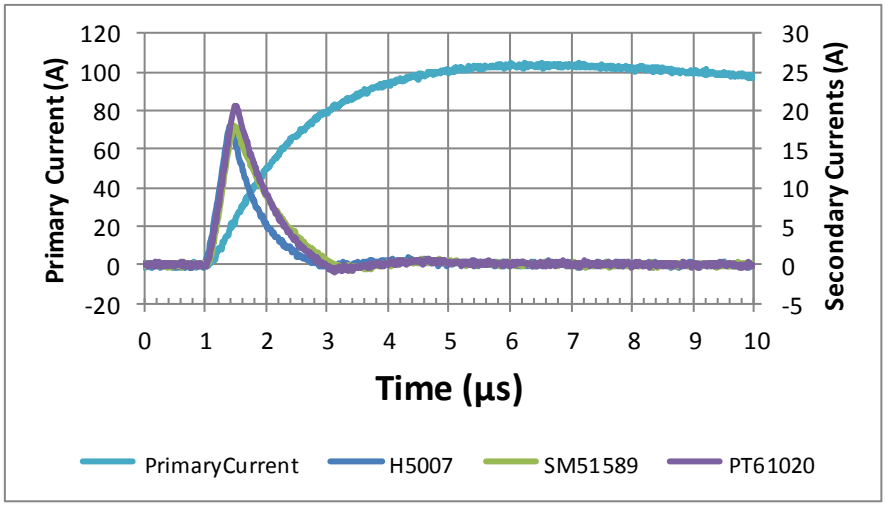


Figure 10b. Primary and Secondary Currents with 100 Ω Load in Parallel with a 5 V TVS Diode

From this data we can see that the transformer will play an important role in protecting the ethernet PHY by providing the first line of defense against a surge event. We have established that all three transformers can handle the 100 A peak current on their primary side while significantly reducing the peak current and the duration of the current waveform on their secondary side. However, the transformer cannot do the complete job by itself. Additional protection is required to reduce the total energy that must be absorbed by the PHY that is being protected.

4.2 Transient Current Suppressor (TCS™) Devices

The Bourns® Transient Current Suppressors (TCS™) are comprised of low resistance, fast response current limiters that provide excellent protection for low voltage communication circuits such as those used in GbE applications. The figures below show a test circuit that was designed to evaluate the performance of a TCS™ device and the response of a Model TCS-DL004-250-WH to a voltage ramp input with a slew rate of approximately 1 V/µs.

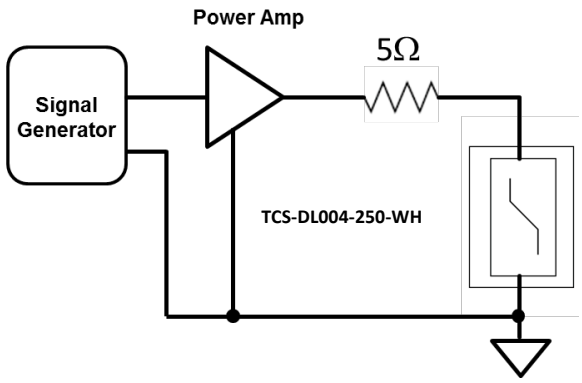


Figure 11. TCS™ Device Test Circuit

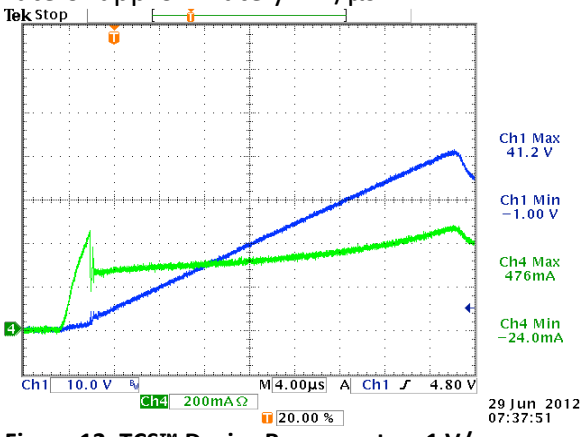


Figure 12. TCS™ Device Response to a 1 V/µs Voltage Ramp

Note that the TCS™ device has a fold-back characteristic. The current folds back to approximately 280 mA after the device is triggered and then slowly increases as the voltage across the device rises. With 40 V across the device, the current through the device is about 476 mA. This characteristic of the current through the device increasing as the voltage across it rises is analogous to how the clamp voltage of a TVS diode increases as the current through the device increases. In a GbE application, the voltage across the TCS™ device would be in the range of 10 to 20 V, depending on the overvoltage protection device used. From figure 12 we can see that the increase in the current through the TCS™ device will be less than 50 mA higher than the fold-back current level with 20 V across the TCS™ device.

4.3 Diodes

For this application we evaluated a 5 V TVS diode and two steering diodes to determine their suitability. The devices tested were the Bourns® Model CDSOD323-T05C (5 V TVS diode), the Bourns® Model CDSOT23-S2004 (two steering diodes per device) and a generic BAV99S (4 diodes per device). The test circuit is shown in figure 13 below and was devised to estimate performance in a GbE application. Figure 14 is a plot of peak voltage vs. current for the three devices. The peak voltage while the diode is turning on is ignored for this graph. We can see that the BAV99S device has the highest dynamic resistance, being about twice that of the other two devices.

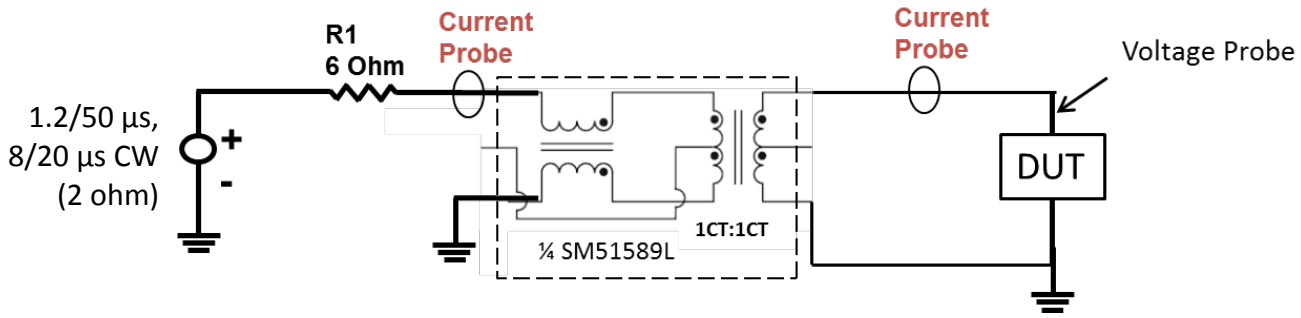


Figure 13. Diode Test Circuit

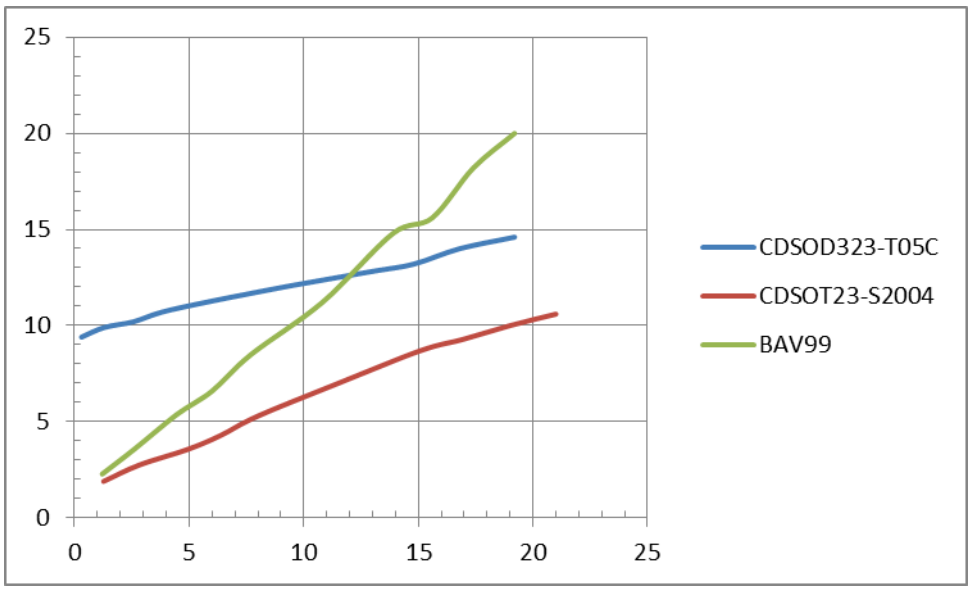
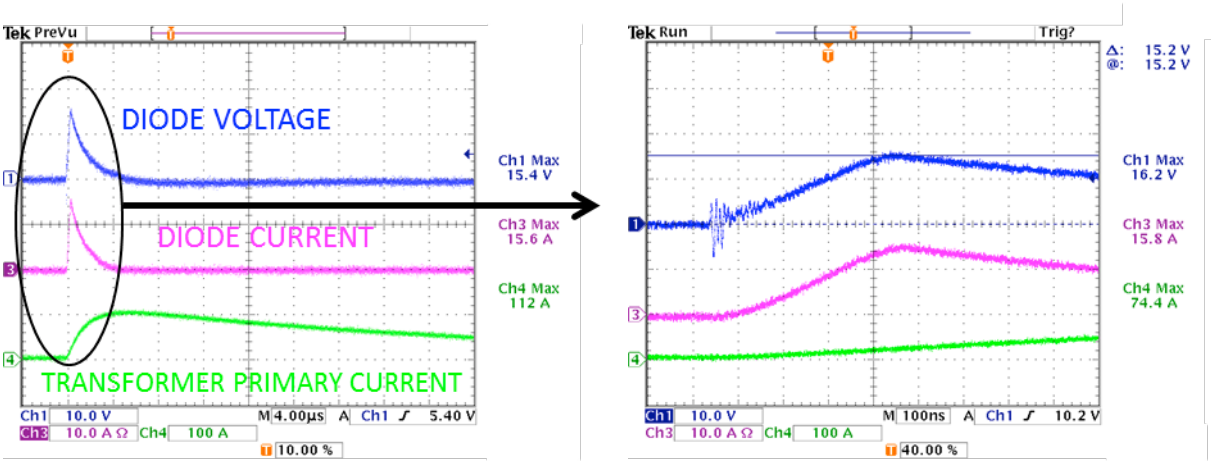


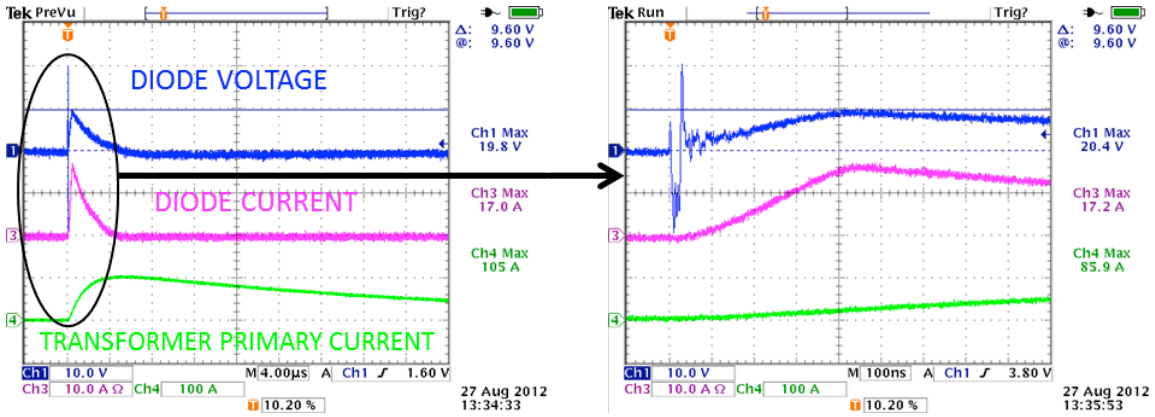
Figure 14. Peak Voltage vs. Peak Current for the Three Diodes Tested

The three diodes do have different turn-on characteristics. The responses of the BAV99S, the Model CDSOT23-S2004 and the Model CDSOD323-T05C when the primary side of the transformer is driven with a peak current of 100 A are shown in figures 15, 16 and 17, respectively. Note that although the voltage across the Model CDSOD323-T05C and CDSOT23-S2004 diodes at the peak current are lower than that of the BAV99S, their turn-on time is somewhat longer, at about 30-40 ns. This results in a peak voltage that is somewhat higher than the diode voltage at the peak current level. The good news is that the maximum voltage rating of a TCS™ device is 40 V so all three of these diodes will easily meet the voltage requirements of our design.



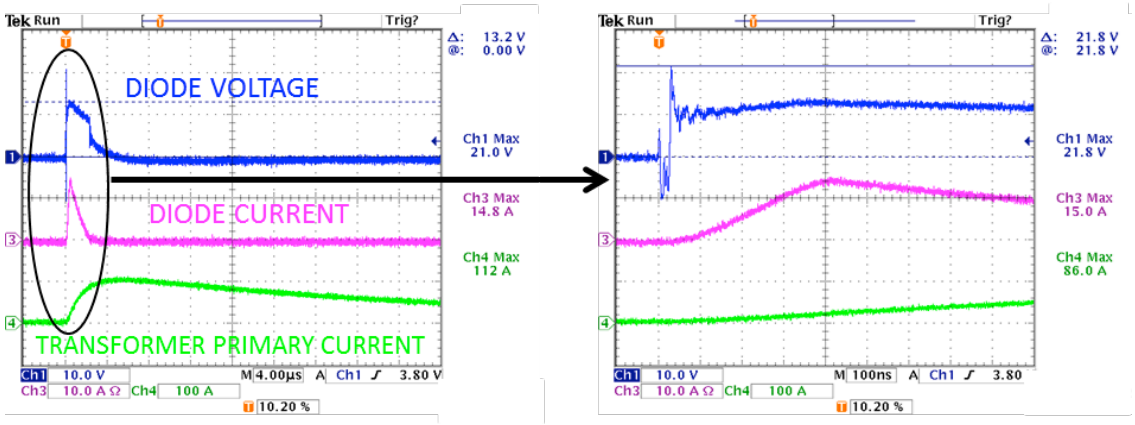
(a) (b)

Figures 15(a) and 15(b). Models SM51589L/BAV99S Response to a 800 V/100 A Combination Wave



(a) (b)

Figures 16(a) and 16(b). Models SM51589L/CDSOT23-S2004 Response to a 800 V/100 A Combination Wave



(a) (b)

Figure 17(a) and 17(b). Models SM51589L/CDSOD323-T05C Response to a 100 A Combination Wave

4.3 Summary of Component Evaluation

We have established the capabilities of the individual components that will be used to protect our Ethernet PHY. Let's put them together as shown in figures 18 through 21 and perform our surge tests. The TVS diode circuit shown in figure 18 will be used to establish a baseline, since it is a topology that is currently in use. The remaining three circuits will be evaluated and the test results will be compared to the first protection circuit as well as to each other.

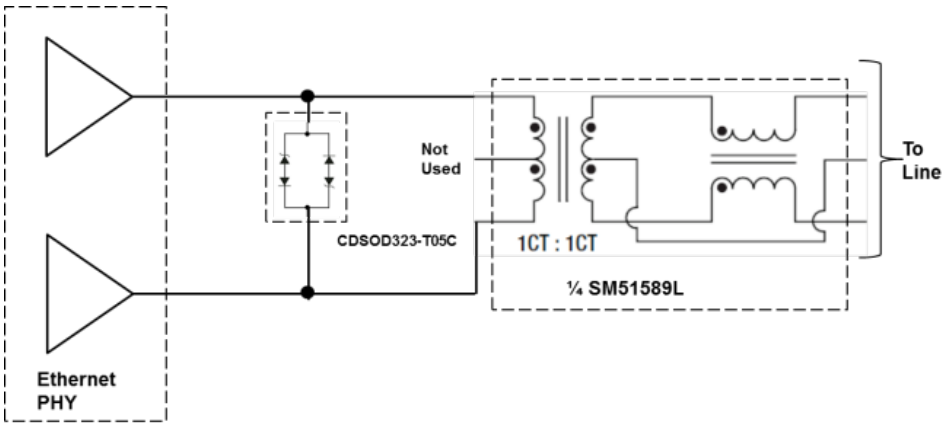


Figure 18. Bidirectional TVS Diode Protection Circuit

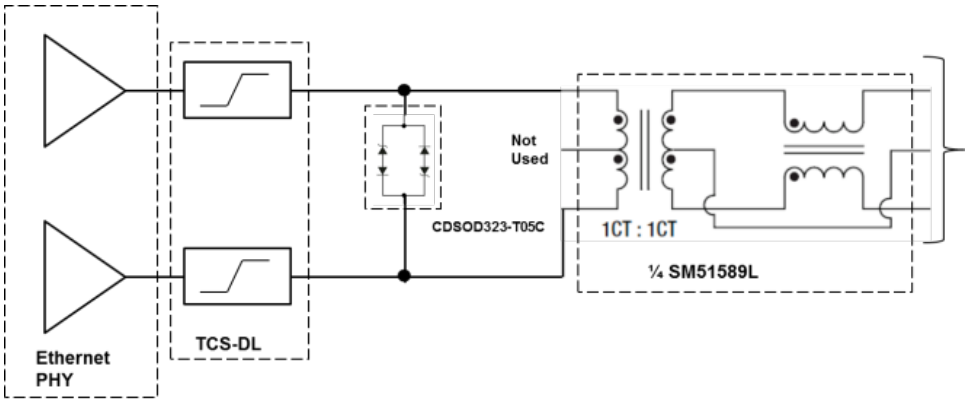


Figure 19. TCS™ Device and Bidirectional TVS Diode Protection Circuit

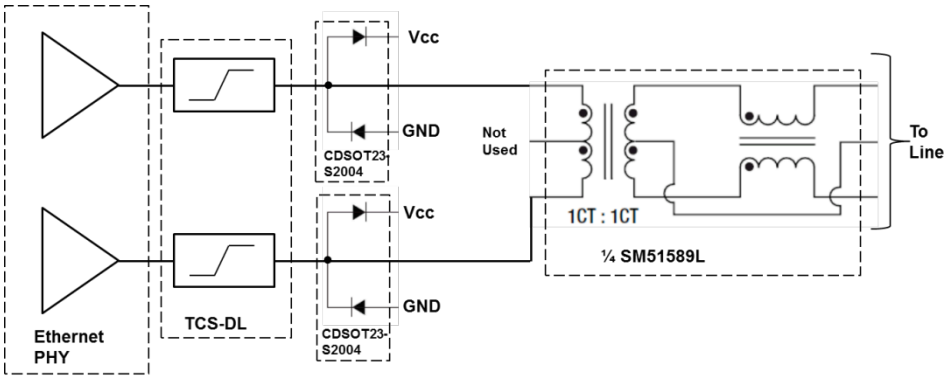


Figure 20. TCS™ Device and Steering Diode Protection Circuit #1

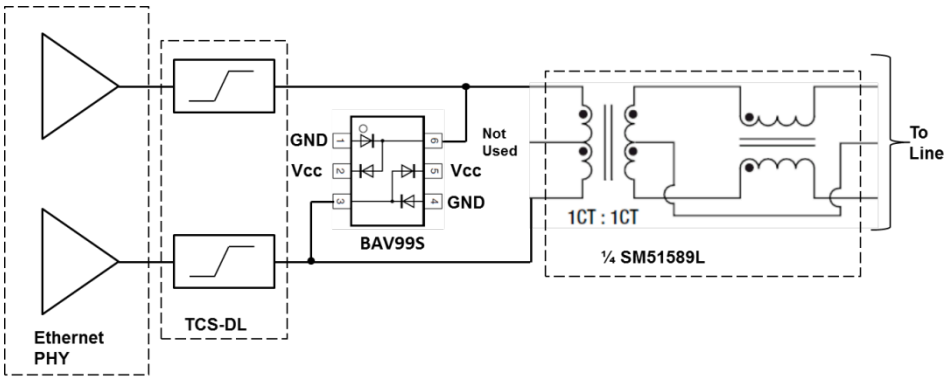


Figure 21. TCS™ Device and Steering Diode Protection Circuit #2

5.0 Surge Tests on GbE Solutions

Three different differential surge tests were performed on each of the four designs shown in figures 18 through 21: the 1.2/50 µs (voltage), 8/20 µs (current) combination wave test, the 10/700 µs voltage waveform test and the 2/10 µs voltage waveform test.

5.1 1.2/50 µs, 8/20 µs Combination Wave Test

The evaluation circuits shown in figures 18, 19, 20 and 21 were tested in accordance with GR - 1089-Core-Issue 6 for port type 4. The test setup for the metallic (differential) test is shown in figure 22. For the differential (metallic) test, the standard (surge test number 12 in table 4-2) calls out using an external 6 ohm resistor in series with the fault source which has an internal output resistance of 2 ohms. The peak surge voltage for the test is 800 V, giving us a peak current of 100 A. From our evaluation of the transformers we saw that they act like very good filters to reduce the peak current by about a factor of four to five and also reduce the transient duration to 2 µs or less when the secondary is loaded with one of our overvoltage protection devices.

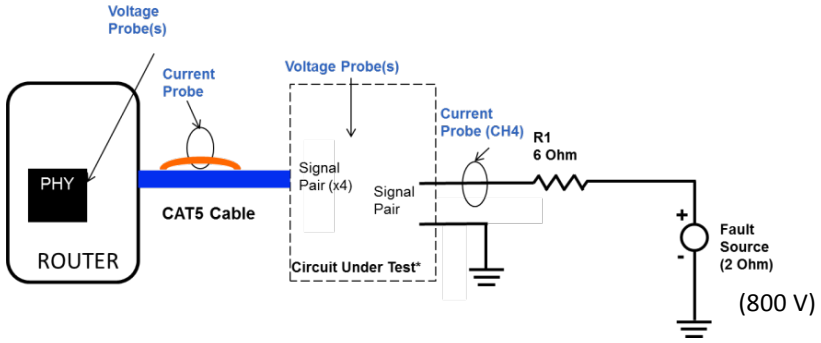


Figure 22. Combination Wave Test Setup

5.1.1 TVS Diode Protection Circuit Evaluation (See Figure 1)

The oscilloscope waveforms in figure 23 shows the performance of the TVS diode protection circuit shown in figure 18 when subjected to the 800 V combination waveform. Note that the peak current and voltage seen by the PHY are ~4 A and ~12.4 V, respectively. An estimate of the energy absorbed by the PHY is ~54 microjoules (3 A x 9 V x 2 µs).

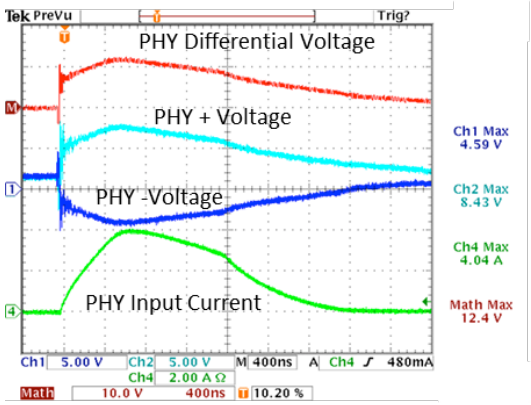


Figure 23. Performance of the TVS Diode Protection Circuit

5.1.2 TCS™ Device/TVS Diode Protection Circuit Evaluation (See Figure 19)

The waveforms in figures 24 and 25 show the performance of the TCS™ device/TVS diode circuit of figure 19 when subjected to the combination wave. While the peak voltage across the TVS diode was just over 15 V the voltage across the PHY inputs is 5.2 V after the initial peak. The current into the PHY is reduced to approximately 275 mA after the initial peak of about 571 mA. The voltage and current levels are significantly reduced compared to the TVS diode only design. An estimate of the energy absorbed by the PHY is ~3 microjoules (0.275 A x 5.2 V x 2 µs).

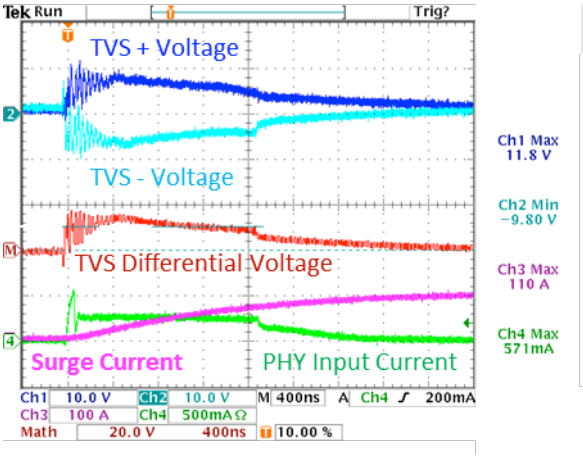


Figure 24. Performance of TCS™ Device/TVS Diode

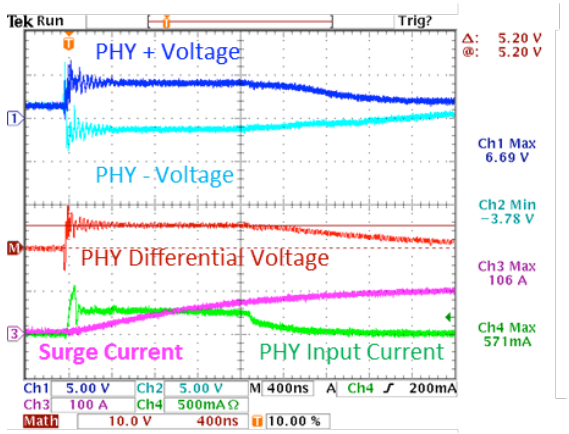


Figure 25. Performance of the TCS™ Device/TVS Diode Protection Circuit

5.1.3 TCS™ Device/Model CDSOT23-S2004 Protection Circuit Evaluation (See Figure 20)

The waveforms in figures 26 and 27 show the performance of the TCS™ device using Model CDSOT23-S2004 diodes as clamps to the 3.3 V power supply and ground (see figure 20) when subjected to the combination waveform. Note that although the differential clamp voltage level on the transformer side of the TCS™ device is higher than in the previous case (23.6 V vs. ~15 V), the voltage and current stress on the PHY are almost identical. An estimate of the energy absorbed by the PHY is ~3 microjoules (0.275 A x 5.2 V x 2 µs).

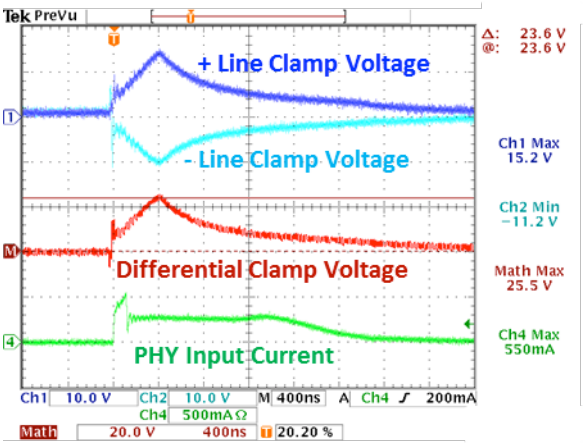


Figure 26. Clamp Diode Voltages for Circuit Shown in Figure 20

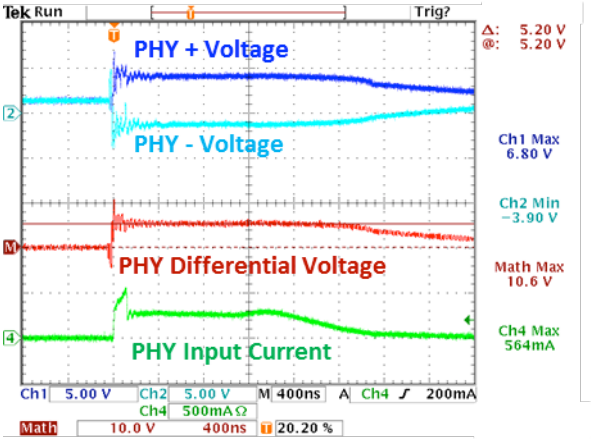


Figure 27. PHY Voltage and Current for TCS™/Clamp Diode Circuit Shown in Figure 20

5.1.4 TCS™ Device/BAV99S Protection Circuit Evaluation (See Figure 21)

The waveforms in figures 28 and 29 show the performance of the TCS™ device using BAV99S diodes as clamps to the 3.3 V power supply and ground as shown in figure 21. Again, note that although the differential clamp voltage level is higher than in the previous two cases, the voltage and current stress on the PHY is about the same. With 34 V across the lines on the transformer side of the TCS™ device, the differential voltage across the PHY inputs is only 5.4 V. This is a good example of the voltage isolation that the TCS™ device provides. An estimate of the energy absorbed by the PHY is ~3 microjoules (0.275 A x 5.4 V x 2 µs).

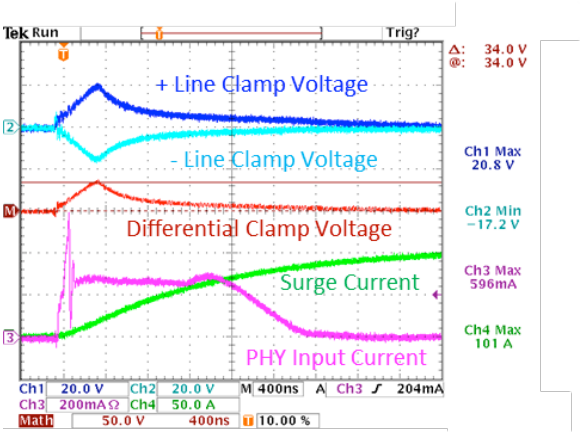


Figure 28. Clamp Diode Voltages for Circuit Shown in Figure 21

21

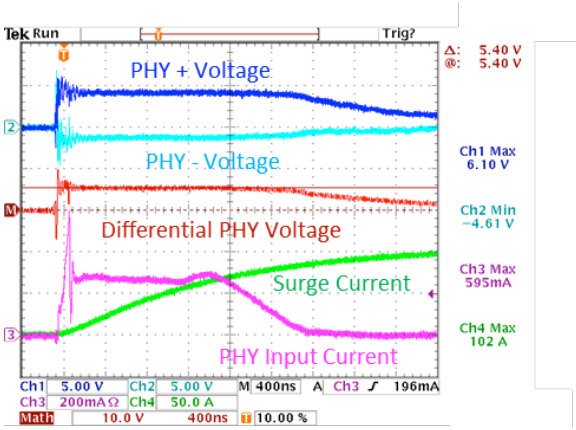


Figure 29. Performance of TCS™ Device/Clamp Diode Circuit Shown in Figure 21

5.1.5 Combination Wave Test Results Summary

A summary of the combination wave testing is shown in table 1. The reduced stress on the PHY afforded by the TCS™ device designs is quite dramatic. It helps provide a very robust design that will minimize any concerns regarding the variation in robustness of ethernet PHYs in a production environment.

Table 1. Summary of 1.2/50, 8/20 CW Test Results

Test	Protection Circuit	Diode Clamp Differential Voltage (V)	PHY Differential Input Voltage (V)	PHY Input Current	Estimate of Energy Absorbed by PHY (µJ)
Differential Surge Test per GR-1089-CORE-ISSUE 6 (800 V/100 A)	Figure 18. TVS Diode Only	12.4	12.4 (same)	4 A peak	54
	Figure 19. TVS Diode with TCS™ Device	~15	<6	<300 mA*	3
	Figure 20. Model CDSOT23-S2004 with TCS™ Device	23.6	<6	<300 mA*	3
	Figure 21. BAV99S with TCS™ Device	34	<6	<300 mA*	3

* After initial peak

5.2 10/700 µs Voltage Waveform Test

The evaluation circuits shown in figures 18, 19, 20 and 21 were tested in accordance with ITU-T K.21. The test setup for the metallic (differential) test is shown in figure 30. The source impedance of the surge generator is approximately 40 Ohms.

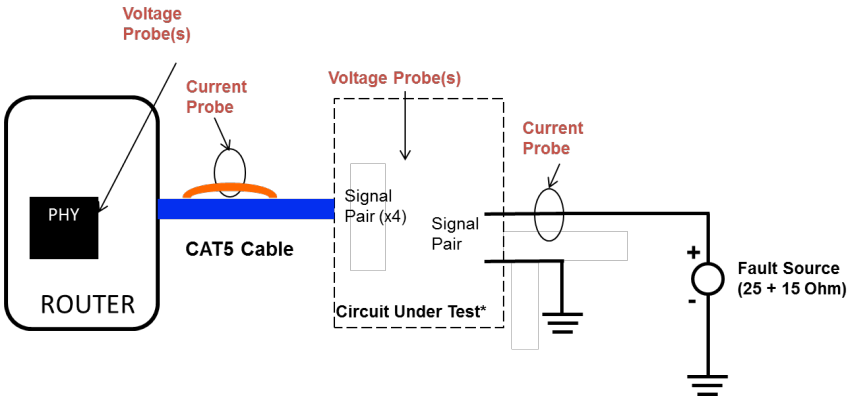


Figure 30. Test Setup for 10/700 µs Differential Surge Test per ITU.k21

5.2.1 TVS Diode Protection Circuit Evaluation (See Figure 18)

The oscilloscope waveforms in figure 31 show the performance of the TVS diode protection circuit shown in figure 18 when subjected to the 4 kV 10/700 µs surge voltage waveform. Note that the peak current and voltage seen by the PHY are ~3.2 A and ~10.4 V, respectively. These levels are slightly lower than those incurred when the design was subjected to the combination wave test in section 4.1.1. This is due primarily to the fact that the rise time of input waveform is slower. An estimate of the energy absorbed by the PHY is ~41 microjoules (2 A x 8.5 V x 2.4 µs).

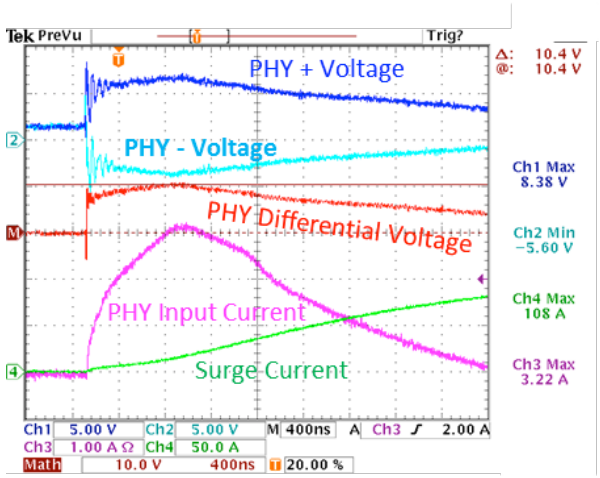


Figure 31. 4 kV, 10/700 µs TVS Diode Design Surge Performance

5.2.2 TCS™ Device/TVS Diode Protection Circuit Evaluation (See Figure 19)

The waveforms in figures 32 and 33 show the performance of the TVS diode/TCS™ device circuit shown in figure 19 to a 10/700 µs surge voltage waveform. While the peak voltage across the TVS diode was just over 12 V after the initial spike of ~16 V, the voltage across the PHY inputs is less than 6 V after the initial peak. The current into the PHY is reduced to approximately 275 mA after the initial peak of about 530 mA. The voltage and current levels that the PHY is subjected to are reduced by about 50 % and 90 %, respectively, compared to the TVS diode only design. An estimate of the energy absorbed by the PHY is ~3.6 microjoules (0.275 A x 5.2 V x 2.5 µs).

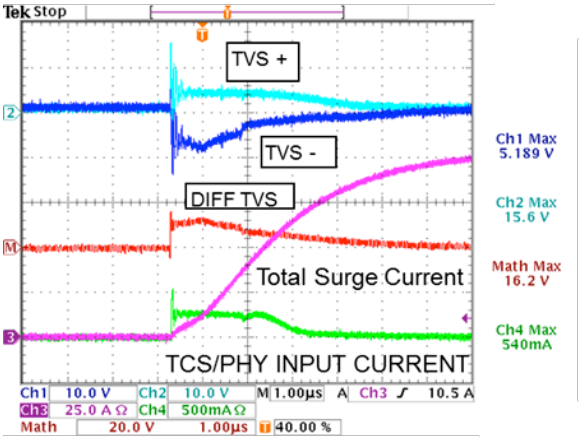


Figure 32. 4 kV, 10/700 µs TVS Diode/TCS™ Device Design Surge Performance

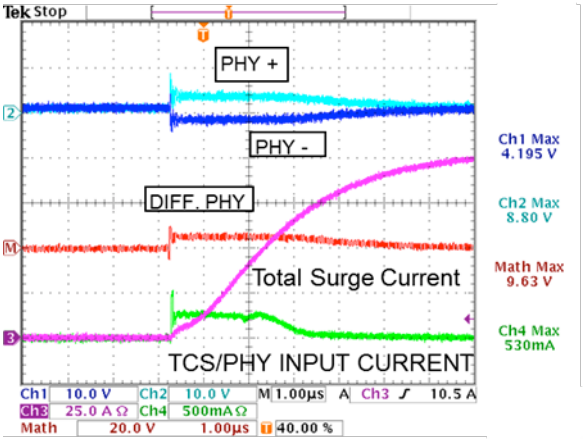


Figure 33. 4 kV, 10/700 µs TVS Diode/TCS™ Device Design Surge Performance

5.2.3 TCS™ Device/Model CDSOT23-S2004 Protection Circuit Evaluation (See Figure 20)

The waveforms in figures 34 and 35 show the performance of the TCS™ device using Model CDSOT23-S2004 diodes as clamps to the 3.3 V power supply and ground (see figure 20) when subjected to a 4 kV, 10/700 µs voltage waveform. Note that although the clamp voltage levels on the transformer side of the TCS™ device are higher than in the previous case, the voltage and current stress on the PHY are almost identical at 5.2 V and approximately 275 mA. An estimate of the energy absorbed by the PHY is ~3.6 microjoules (0.275 A x 5.2 V x 2.5 µs).

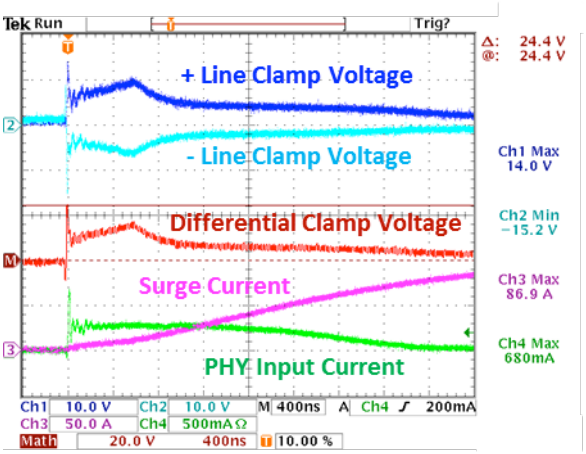


Figure 34. 4 kV, 10/700 µs TCS™ Device/Model CDSOT23-S2004 Design Surge Performance

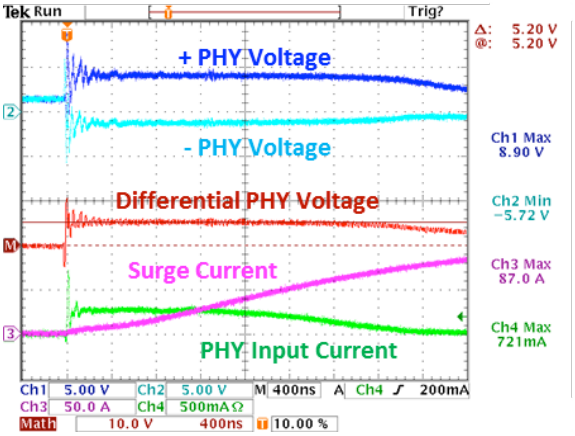


Figure 35. 4kV, 10/700 µs TCS™ Device/Model CDSOT23-S2004 Design Surge Performance

5.2.4 TCS™ Device/BAV99S Protection Circuit Evaluation (See Figure 21)

The waveforms in figures 36 and 37 show the performance of the TCS™ device, using BAV99S diodes as clamps to the 3.3 V power supply and ground (see figure 21), when subjected to a 4 kV, 10/700 µs voltage waveform. Note that although the clamp voltage levels on the transformer side of the TCS™ device are higher than in the TCS™ Device/Model CDSOT23-S2004 in our previous case (21 V vs. 16 V, ignoring initial overshoot), the voltage and current stress on the PHY are almost identical at 5.4 V and approximately 275 mA. An estimate of the energy absorbed by the PHY is ~3.7 microjoules (0.275 A x 5.4 V x 2.5 µs).

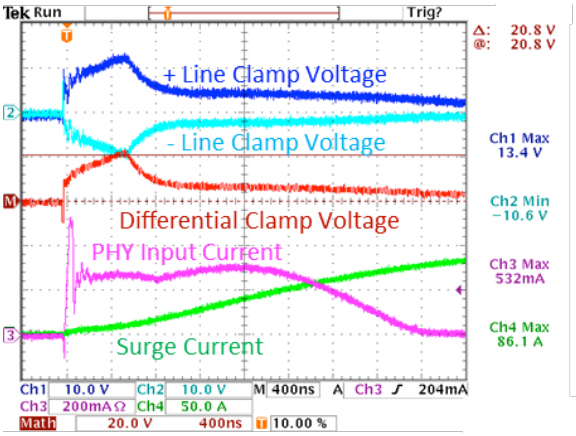


Figure 36. 4 kV, 10/700 µs TCS™ Device/BAV99S Design Surge Performance

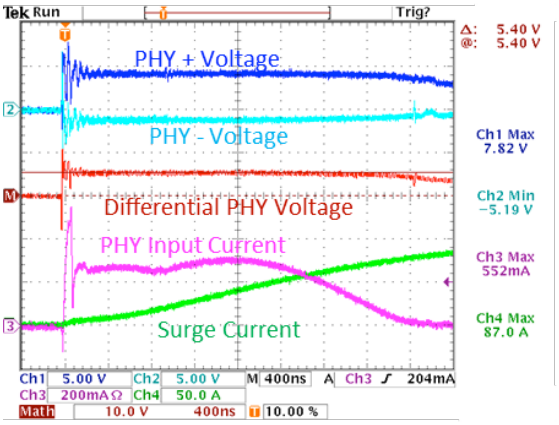


Figure 37. 4 kV, 10/700 µs TCS™ Device/BAV99S Design Surge Performance

5.2.5 4 kV, 10/700 µs Test Results Summary

A summary of the 4 kV, 10/700 µs testing is shown in table 2. The reduced stress on the PHY afforded by the TCS™ device designs is quite dramatic. It helps provide a very robust design that will minimize any concerns regarding the variation in robustness of ethernet PHYs in a production environment.

Table 2. Summary of 10/700 µs Voltage Waveform Test Results.

Test	Protection Circuit	Diode Clamp Differential Voltage (V)	PHY Differential Input Voltage(V)	PHY Input Current	Estimate of Energy Absorbed by PHY (µJ)
Differential Surge Test per ITU-T K.21 (4 kV/100 A)	Figure 18. TVS Diode Only	10.4	10.4 (same)	3.2 A peak	41
	Figure 19. TVS Diode with TCS™ Device	~12	<6	<300 mA*	3.6
	Figure 20. Model CDSOT23-S2004 with TCS™ Device	16*	<6	<300 mA*	3.6
	Figure 21. BAV99S with TCS™ Device	21	<6	<300 mA*	3.7

* After initial peak

5.3 2/10 µs (800 V/100 A) Voltage Waveform Test

The evaluation circuits shown in figures 18, 19, 20 and 21 were tested in accordance with GR1089-CORE-ISSUE 6 for the 2/10 µs voltage waveform test which can be used in place of the combination wave test. The test setup for the metallic (differential) test is shown in figure 38.

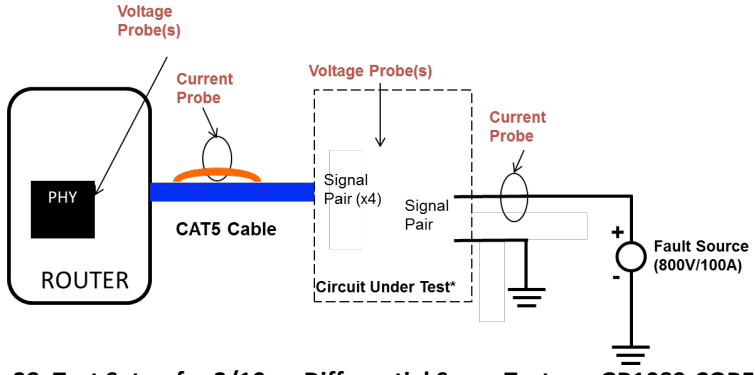


Figure 38. Test Setup for 2/10 µs Differential Surge Test per GR1089-CORE-ISSUE 6

5.3.1 TVS Diode Protection Circuit Evaluation (See Figure 18)

The oscilloscope waveforms in figure 39 show the performance of the TVS diode protection circuit shown in figure 18 when subjected to the 2/10 µs surge voltage waveform. Note that the peak current and voltage seen by the PHY are ~4.4 A and ~12.4 V, respectively. These levels are slightly higher than those incurred in the previous tests on this design. This is due primarily to the fact that the rise time of input waveform is faster. An estimate of the energy absorbed by the PHY is ~54 microjoules (3 A x 9 V x 2 µs).

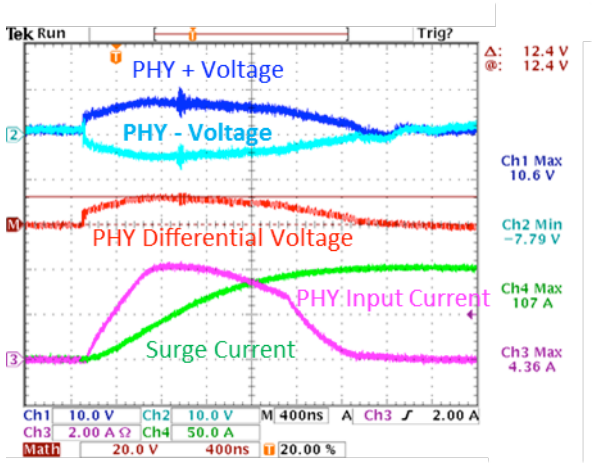


Figure 39. 800 V, 2/10 µs TVS Diode Design Surge Performance

5.3.2 TCS™ Device/TVS Diode Protection Circuit Evaluation (See Figure 19)

The waveforms in figures 40 and 41 show the performance of the TVS diode/TCS™ device circuit shown in figure 19 to a 2/10 µs surge voltage waveform. While the peak voltage across the TVS diode is 15.6 V, the voltage across the PHY inputs is less than 6 V after the initial peak. The current into the PHY is reduced to approximately 275 mA after the initial peak of about 570 mA. The voltage and current levels that the PHY is subjected to are reduced by more than 50 % and 90 %, respectively, compared to the TVS diode only design. An estimate of the energy absorbed by the PHY is ~2.4 microjoules (0.275 A x 5.5 V x 1.6 µs).

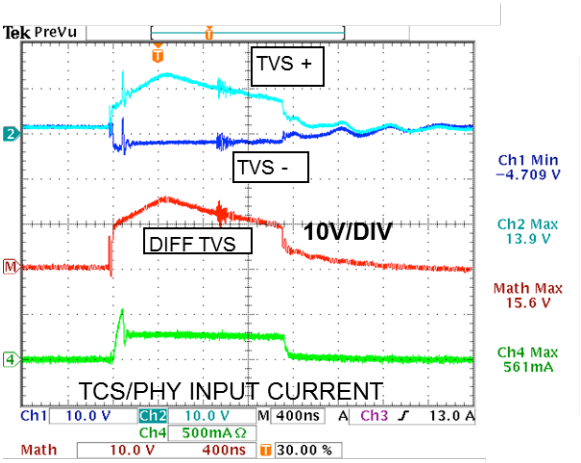


Figure 40. 800 V, 2/10 µs TVS Diode/TCS™ Device Design Surge Performance

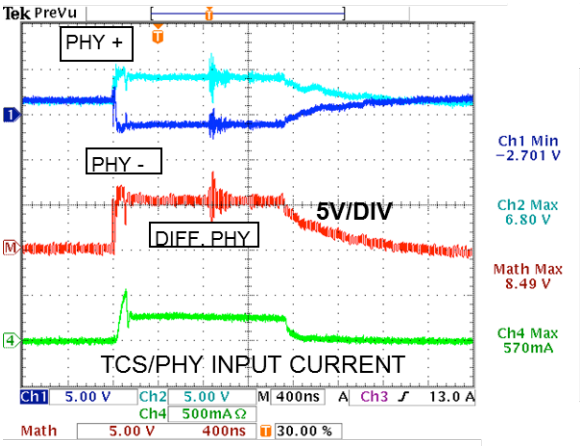


Figure 41. 800 V, 2/10 µs TVS Diode/TCS™ Device Design Surge Performance

5.3.3 TCS™ Device/Model CDSOT23-S2004 Protection Circuit Evaluation (See Figure 20)

The waveforms in figures 42 and 43 show the performance of the TCS™ Device/Model CDSOT23-S2004 circuit shown in figure 20 to a 2/10 µs surge voltage waveform. While the peak differential voltage across the clamp diodes is 25.6 V, the voltage across the PHY inputs is 5.6 V after the initial peak. The current into the PHY is reduced to approximately 275 mA after the initial peak of about 580 mA. The voltage and current levels that the PHY is subjected to are reduced by about 50 % and 90 %, respectively, compared to the TVS diode only design. An estimate of the energy absorbed by the PHY is ~3.1 microjoules (0.275 A x 5.6 V x 2 µs).

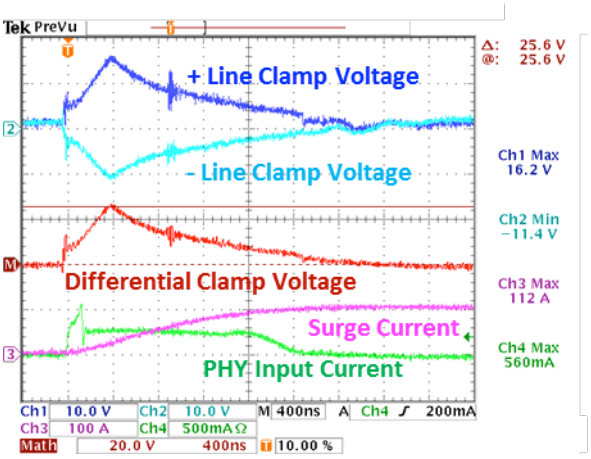


Figure 42. 800 V, 2/10 µs TCS™ Device/Model CDSOT23-S2004 Design Surge Performance

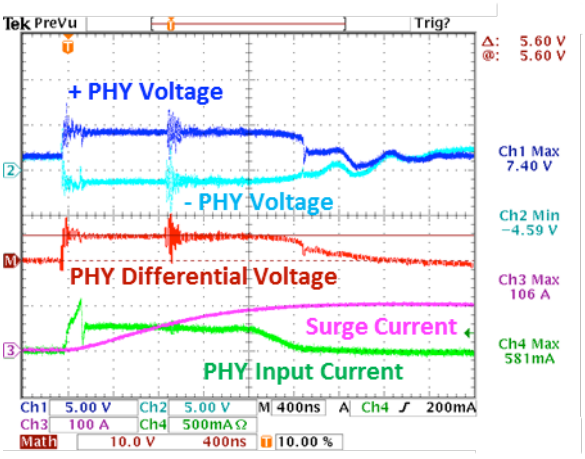


Figure 43. 800 V, 2/10 µs TCS™ Device/Model CDSOT23-S2004 Design Surge Performance

5.3.4 TCS™ Device/BAV99S Protection Circuit Evaluation (See Figure 21)

The waveforms in figures 44 and 45 show the performance of the TCS™ device/BAV99S circuit shown in figure 21 to a 2/10 µs surge voltage waveform. While the peak differential voltage across the clamp diodes is 36 V, the voltage across the PHY inputs is 5.2 V after the initial peak. The current into the PHY is reduced to approximately 275 mA after the initial peak of about 588 mA. The voltage and current levels that the PHY is subjected to are reduced by more than 50 % and 90 %, respectively, compared to the TVS diode only design. An estimate of the energy absorbed by the PHY is a ~2.9 microjoules (0.275 A x 5.2 V x 2 µs).

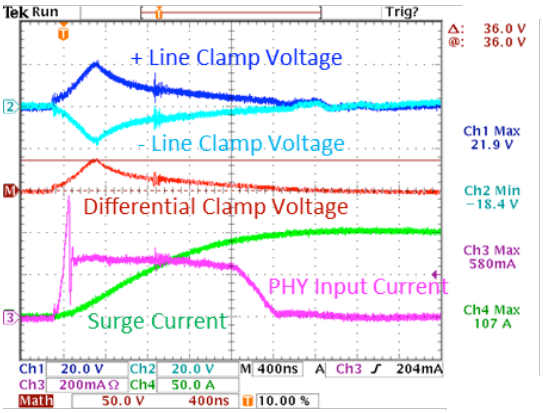


Figure 44. 800 V, 2/10 µs TCS™ Device/BAV99S Design Surge Performance

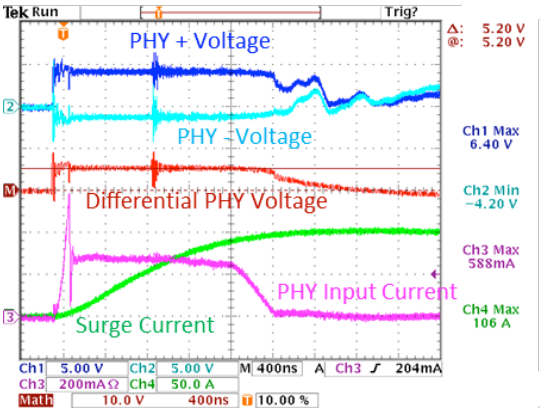


Figure 45. 800 V, 2/10 µs TCS™ Device/BAV99S Design Surge Performance

5.3.5 800 V, 2/10 µs Test Results Summary

A summary of the 800 V, 2/10 µs testing is shown in table 3 below. The reduced stress on the PHY afforded by the TCS™ device design is quite dramatic. It helps provide a very robust design that will minimize any concerns regarding the variation in robustness of ethernet PHYs in a production environment. Notice that the diode clamp voltage levels for this waveform are higher than for either of the other two waveforms. This is due primarily to the faster rise time of the surge waveform.

Table 3. Summary of 2/10 µs Voltage Waveform Test Results

Test	Protection Circuit	Diode Clamp Differential Voltage (V)	PHY Differential Input Voltage (V)	PHY Input Current	Estimate of Energy Absorbed by PHY (µJ)
2/10 µs Differential Surge Test per GR1089-CORE-ISSUE 6 (800 V/100 A)	Figure 18. TVS Diode Only	12.4	12.4 (same)	4.4 A peak	54
	Figure 19. TVS Diode with TCS™ Device	15.6	<6	<300 mA*	2.4
	Figure 20. Model CDSOT23-S2004 with TCS™ Device	25.6	<6	<300 mA*	3.1
	Figure 21. BAV99S with TCS™ Device	36	<6	<300 mA*	2.9

* After initial peak

6 GbE Signal Performance Evaluation

IEEE Standard 802.3-2008 (Rev. 26 Dec. 2008) requires specific signal performance characteristics for a GbE signal. Two of the tests that would be pertinent to the effect of using a TCS™ device are the signal template and amplitude tests. These tests were performed on the circuits shown in figures 18 and 19 with one modification. The Ethernet transformer used was a Bourns® Model PT61020L transformer instead of a Bourns® Model SM51589L transformer. The basic test setup is shown in figure 46. The circuits being evaluated are on a separate circuit board (normally, the design would be located on the PHY board) so there are more parasitics involved because of the extra connectors and cables as well as the longer trace lengths involved. The effects of these parasitics would be reduced if the circuit was designed into the PHY board.

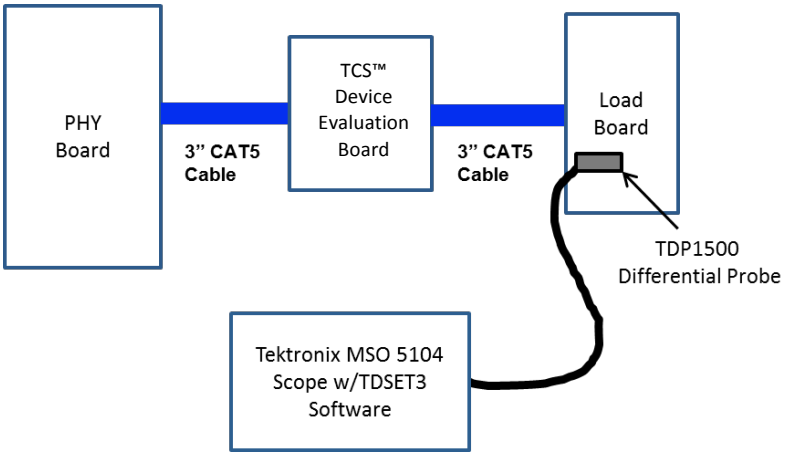


Figure 46. GbE Signal Amplitude and Template Test Setup

The PHY was set to test mode 1 (transmit waveform test) for all the tests that were performed. The test waveform is defined in figure 40-19 of the IEEE802.3-2008 specification and is shown in figure 47. The differential waveform at the load was measured using a 1.5 GHz differential probe and a 1 GHz oscilloscope. The waveform was analyzed using Tektronix TDSET3 analysis software. All of the template and amplitude tests were performed on both designs. Both designs passed all the tests performed. Some of the data is presented in the following paragraphs so that the performance of the TCS™ device can be understood.

The amplitude results at points A and B of the test waveform for both circuits are shown in table 4. Note that the addition of the TCS™ device accounts for less than 15 mV (<0.2 dB) of signal loss in comparison to the TVS diode only design. When we compare this attenuation to that of a typical CAT 5 cable (approximately 22 dB per 100 meters at 100 MHz), it is the equivalent of less than 1 meter of cable.

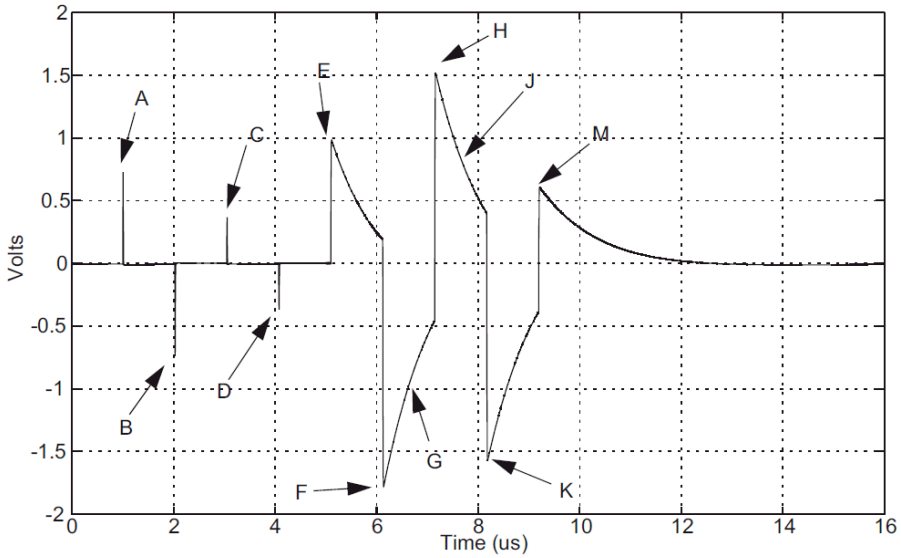


Figure 47. Example of Transmitter Test Mode 1 Waveform (1 Cycle)

Source: IEEE Standards Association (IEEE 802.3™: ETHERNET)

The oscilloscope waveforms in figures 48 and 49 show the template test results at point A for the figure 18 and figure 19 design, respectively. Figures 50 and 51 show the waveforms for both designs at point F of the test waveform. The results at the other evaluation points (B, C, D, and G) are similar. The results for the other three line pairs closely resemble those of line pair 1.

Table 4. Amplitude Test Results

Line Pair	Point	Figure 18 Schematic: Transformer and TVS diode (mV)	% Peak Voltage Difference Between Points A and B	Figure 19 Schematic: Model TCS-DL004-250-WH, Transformer and TVS diode (mV)	% Peak Voltage Difference Between Points A and B	Loss due to TCS™ Device		
						mV	%	dB
1	A	768.7	0.73 %	754.1	0.49 %	14.6	1.9 %	-0.17
	B	763.1		750.4		12.7	1.7 %	-0.15
2	A	760.7	0.50 %	746.5	0.44 %	14.2	1.9 %	-0.16
	B	756.9		743.2		13.7	1.8 %	-0.16
3	A	772.4	0.06 %	759.9	0.13 %	12.5	1.6 %	-0.14
	B	771.9		760.9		11.0	1.4 %	-0.12
4	A	768.7	0.88 %	754.5	0.76 %	14.2	1.8 %	-0.16
	B	762.0		748.8		13.2	1.7 %	-0.15

Table 4 Notes:

1. The required amplitude range for the signal at points A and B is 670 mV to 820 mV.
2. The % peak voltage difference between points A and B must be <1 %.

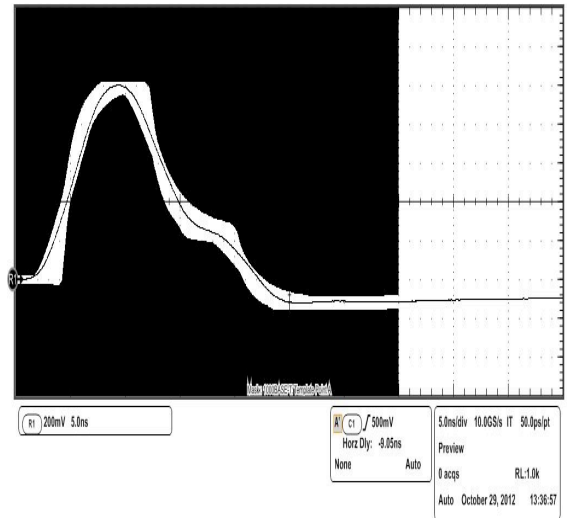


Figure 48. Figure 18, Line Pair 1 Template Test Result @ Pt. A

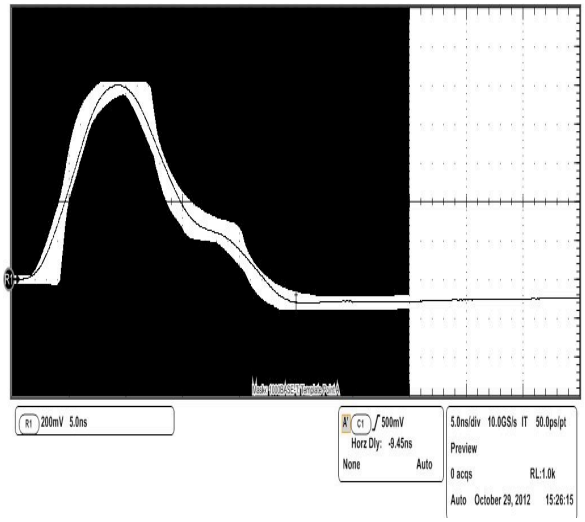


Figure 49. Figure 19, Line Pair 1 Template Test Result @ Pt. A

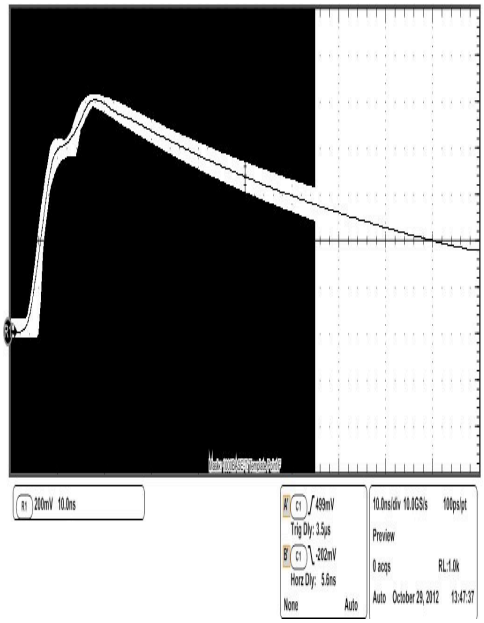


Figure 50. Figure 18, Line Pair 1 Template Test Result @ Pt. F

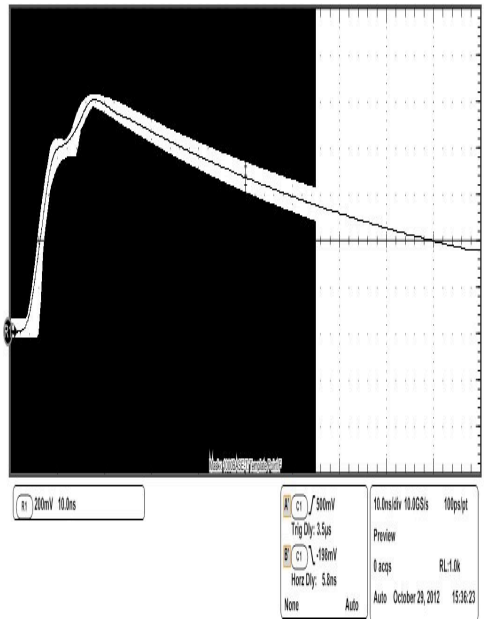


Figure 51. Figure 19, Line Pair 1 Template Test Result @ Pt. F

In conclusion, the TCS™ device design meets the signal template and amplitude requirements of IEEE802.3-2008 and has minimal impact on the quality of the GbE signal in comparison to the TVS diode only design.

7 Conclusion

The new Bourns® Transient Current Suppressor (TCS™) devices enable the creation of a protection circuit that closely resembles the performance of an ideal diode. When coordinated with appropriate overvoltage protection and the ESD structure of the protected device, the TCS™ device significantly enhances the protection level achievable by a TVS diode alone. This capability was clearly demonstrated in our GbE application surge testing.

The TCS™ device based GbE protection circuits shown in figures 19, 20 and 21 significantly reduce the energy that the Ethernet PHY must absorb (by more than 90 %) during a surge transient compared to the TVS diode only design shown in figure 18. Although the clamp voltage levels of these three designs vary significantly, the TCS™ device effectively isolated the PHY from these higher clamp voltages. The voltage at the inputs to the PHY (<6 V for all three designs) is determined by its response to the limited current that passes through the TCS™ device. Using the Model TCS-DL004-250-WH limits the current to <300 mA for all three surge waveforms which is significantly less than the 3.2 to 4.4 A the PHY must sink or source when using the TVS diode only design shown in figure 18.

Signal template and amplitude tests were performed per IEEE802.3-2008 on the circuit topologies shown in figures 18 and 19. Both designs met the requirements of the standard. The addition of a TCS™ device to the design had minimal impact on the quality of the test signal.

The Bourns® Model TCS-DL-250-WH offers superior protection while not compromising signal quality in any meaningful way. The use of the TCS™ device allows the use of a less rigid clamp device/design without compromising the level of protection provided.