BOURNS®

Circuit Protection Division

July, 2005

Bourns Manufacturers Representatives
Corporate Distributor Product Managers
Americas Sales Team
Asia Sales Team
Europe Sales Team

BOURNS® CIRCUIT PROTECTION Update

Thyristor Surge Protector Product Change Notification

PCN Tracking Number 37 - Chip Metallization Change

Recent advances in underbump metallization technology afford the opportunity for Bourns to change the wafer metallization system used on all SMA and SMB packaged products. Bourns wafers designed for solder die attach are manufactured with a multilayer metal system to achieve low contact resistance, high strength, good solderability and long application life. In the new system, the metallization deposition process will change from vacuum deposition only, to a combination of vacuum deposition and electroless plating. The deposition processes and thickness of each layer are shown in the table.

	Current		Future	
	Deposition	**Thickness**	**Deposition**	**Thickness**
Aluminum	Vacuum	6 microns	Vacuum	6 microns
Titanium	Vacuum	0.15 microns	Not present	N/A
Nickel	Vacuum	0.45 microns	Plating	2.0 - 5.0 microns
Gold	Vacuum	0.04 microns	Plating	0.04 - 0.10 microns

In vacuum metallizing, the titanium layer is necessary as an adhesive layer between nickel and aluminum. The nickel-plating process has high adhesion to aluminum so the titanium layer is no longer required.

Products Affected by the Change:

Initially, all overvoltage protection products assembled in the SMA and SMB are affected. Products with package code suffixes of AJ, AJR, BJ and BJR will be changed. For lead (Pb) free products, the corresponding codes are AJ-S, AJR-S, BJ-S and BJR-S. Products in other packages will be converted later.

Surface Mount Packages

Existing Part No	Package	Lead Free	RoHS Compliant	Lead Free Product Part Number Suffix -S or S
TISP Products				
TISP4xxxL1AJR	SMA	Yes	Yes	TISP4xxxL1AJR-S
TISP4xxxL3AJR	SMA	Yes	Yes	TISP4xxxL3AJR-S
TISP4xxxM3AJR	SMA	Yes	Yes	TISP4xxxM3AJR-S
TISP43xxMMAJR	SMA	Yes	Yes	TISP43xxMMAJR-S
TISP4xxxL1BJR	SMB	Yes	Yes	TISP4xxxL1BJR-S
TISP4xxxL3BJR	SMB	Yes	Yes	TISP4xxxL3BJR-S
TISP4xxxM3BJR	SMB	Yes	Yes	TISP4xxxM3BJR-S
TISP43xxMMBJR	SMB	Yes	Yes	TISP43xxMMBJR-S
TISP4xxxH1BJR	SMB	Yes	Yes	TISP4xxxH1BJR-S
TISP4xxxH3BJR	SMB	Yes	Yes	TISP4xxxH3BJR-S
TISP4xxxH4BJR	SMB	Yes	Yes	TISP4xxxH4BJR-S
TISP4AxxxH3BJR	SMB	Yes	Yes	TISP4AxxxH3BJRS
TISP4CxxxxH3BJR	SMB	Yes	Yes	TISP4CxxxH3BJRS
TISP5xxxH3BJR	SMB	Yes	Yes	TISP5xxxH3BJR-S
TISP1xxxH3BJR	SMB3	Yes	Yes	TISP1xxxH3BJR-S
TISP3xxxT3BJR	SMB3	Yes	Yes	TISP3xxxT3BJR-S

Reason for the Change:
Recent advances in the development of underbump metal systems have indicated that plated metal layers are as reliable as the vacuum-deposited metallization systems currently used.

Product Labeling:
There will be no change to the product labeling.

Identification of the Changed Product:
Bourns maintains traceability back to source wafer lots for all products.

Implementation Date:
Manufacture of wafers with the changed metallization will begin in August 2005. Shipments of finished goods including the metallization changes are expected to commence in September 2005. Existing inventories of wafers manufactured prior to the change will be processed on a FIFO basis. From September 2005, onwards Bourns total shipments of SMA/SMB products will continue to contain wafers manufactured to the existing process until inventory is depleted.

Date Code Product will Include this Processing will be:
0536

Impact on Form, Fit, Function and Reliability:
None

Qualification Plan:
See below.

Last Date of Manufacture of Unchanged Product:
July 2005

Qualification Information as Follows:

TISP4xxxH3BJ & TISP4xxxM3BJ	Chip Metallization Change
Die Technology	Thyristor Overvoltage Protector
Die Name	As Table (Row 2)
Die size (mil)	As Table (Row 3)
Top Metal	Al + NiAu
Back Metal	Al + NiAu
Assembly Site	Shanghai Seefull Electronics Co, PRC
Pins/Package	SMB
Mold Compound	Sumitomo EME 1100H
Die Attach	Solder, Pb >85 %
Bond Wire	Solder Clip (3)
L/F Material	Copper
Marking	Laser
Termination Finish	Matte Sn (Pb Free)

Qualification Samples Taken from Three Wafer Fabrication Lots:

					Test Plan		
					Lot 1	Lot 2	Lot 3
					TW435PQ	TW435PQ	TA230LQ
Stress Test/Conditions (2)	QSS (1)	Standard	Method	SS/Accept	94 x 81	94 x 81	65 x 65
HTRB, 150 °C, 100 V, 1000 h	009-101	MIL STD 883	1015	129/1	129	129	129
85 °C/85 %RH, 50 V, 1000 h	009-102	JEDEC STD 22	A101	129/1	129	129	129
Temperature Cycle - 65/+150 °C, 200 cs	009-104	MIL STD 883	2031	129/1	129	129	129
10/1000 µs Surge	-	GR-1089-CORE	-	16/0	16	16	16
2/10 µs Surge	-	GR-1089-CORE	-	16/0	16	16	16
Bond Strength, 300 g Min. (Note 4)	-	-	-	20/0	20/0	20/0	20/0

Notes:
1. QSS Specifications are Bourns Internal Qualification Standards.
2. Mechanical/Package Requirements qualified by similarity with existing product.
3. SMA and SMB packages are assembled by soldering the chip between a copper lead frame and copper clip.
4. Vertical Pull Test complete.

Stress Test Completion Date:
July 2005